Department of Computer Science and Engineering

Course Name : COMPUTER ORGANIZATION

Course Number : 

Course Designation: Core

Prerequisites : Digital Logic Design

II B Tech – II Semester

(2015-2016)

P. ANJAIAH
Associate Professor
# COMPUTER ORGANIZATION

(COMMON FOR CSE & IT)

(CORE)

II Year B.Tech CSE - II Semester

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**Course Objectives:**

To become familiar in following topics

1. Understand instruction format, life cycle and CPU Architecture and Organization
2. Understanding The Basic Architecture Of Microprocessor With Pin Diagram
3. Understand different types of I/O interfaces with CPU
5. Familiar with The Concepts of Multiprocessor

## SYLLABUS

<table>
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<tr>
<th>Unit – I [TB-1]</th>
<th>Instruction definition, instruction cycle, instruction storage, types of instruction formats (Zero, one, two, three address) addressing modes, mode filed, implied, immediate register, register direct, register indirect, auto increment, decrement, indexed, relative, base address mode, numerical example and problems.</th>
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<td>Unit III [TB-1]</td>
<td>CPU and main memory interface, programming, the basic computer – machine assembly language, assembler, basic, assembly language instructions (ADD, SUB, LOAD, STORE, MOV, CMP, JUMP), micro programmed control, control memory, address sequencing, micro program example, and design of control unit.</td>
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<tr>
<td>Unit IV [TB-1]</td>
<td>I/O Interface: I/O bus and interface modules, I/O versus memory bus. Modes of transfer, example of programmed I/O, interrupt initiated I/O, software considerations, daisy – chaining priority, DMA: DMA controller, DMA transfer, Intel 8089, IOP</td>
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<tr>
<td>Unit V [TB-1]</td>
<td>MULTIPROCESSORS: characteristic of multi processor, interconnection structure,: time shared common bus, multiport memory, cross bar Switch, multistage switching network, introduction to Flynn’s classification: SISD, SIMD, MISD, MIMD (Introduction).</td>
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TEST BOOKS


Reference Books

Websites References

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PROGRAM EDUCATIONAL OBJECTIVES (PEO’s)

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<tr>
<th>PEO</th>
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<tr>
<td>PEO1</td>
<td>The Graduates are employable as software professionals in reputed industries.</td>
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<tr>
<td>PEO2</td>
<td>The Graduates analyze problems by applying the principles of computer science, mathematics and scientific investigation to design and implement industry accepted solutions using latest technologies.</td>
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<tr>
<td>PEO3</td>
<td>The Graduates work productively in supportive and leadership roles on multidisciplinary teams with effective communication and team work skills with high regard to legal and ethical responsibilities.</td>
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<tr>
<td>PEO4</td>
<td>The Graduates embrace lifelong learning to meet ever changing developments in computer science and Engineering.</td>
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PROGRAM OUTCOMES (PO’s)

<table>
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<tr>
<th>PO1</th>
<th>An ability to communicate effectively and work on multidisciplinary teams</th>
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<tr>
<td>PO2</td>
<td>An ability to identify, formulate and solve computer system problems with professional and ethical responsibility.</td>
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<tr>
<td>PO3</td>
<td>A recognition of the need for, and an ability to engage in life-long learning to use the latest techniques, skills and modern engineering tools</td>
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<tr>
<td>PO4</td>
<td>The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental and social context</td>
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<tr>
<td>PO5</td>
<td>An ability to apply knowledge of mathematics, science, and computing to analyze, design and implement solutions to the realistic problems.</td>
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<tr>
<td>PO6</td>
<td>An ability to apply suitable process with the understanding of software development practice.</td>
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Course outcomes:

Upon successful completion of this course, students will be able to:

- CO1. Analyze an instruction-set architecture and propose a suitable data path and control Unit implementation
- CO2. Apply, how instruction pipelining enhances processor performance
- CO3. Design and synthesize new and better architectures
- CO4. Identify the problems in components of computer and can deal with different Computers
- CO5. Work with the Multiprocessor Concepts

MAPPING OF COURSE OUT COMES WITH PO’s & PEO’s

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<td>Ch5,8</td>
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<td>II</td>
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<td>III</td>
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<td>V</td>
<td>Multiprocessors</td>
<td>Ch13</td>
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**Contact classes for Syllabus coverage**

- Tutorial Classes : 05 ; Online Quiz : 1
- Case studies-2hrs (Before 1st Mid Examinations)
- Case studies-2hrs (After 1st Mid Examinations)
- Revision classes :1 per unit

**Number of Hours / lectures available in this Semester / Year**

60
## Lecture Plan

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**Unit-4**

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### Date of Unit Completion & Remarks

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# Unit Wise Assignments (With different Levels of thinking (Blooms Taxonomy))

**Note:** For every question please mention the level of Blooms taxonomy

## Unit – 1

### 1. 

1. A computer uses a memory unit with 256k words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.
   
   a. How many bits are there in the operation code, register code part, and address part?
   
   b. Draw the instruction word format and indicate the number of bits in each part.
   
   c. How many bits are there in the data and address inputs of memory?

### 2. 

The contents of AC in the basic computer is hexadecimal A937 and the initial value of E IS 1. determine the contents of AC, E, PC, AR, and IR in hexadecimal after the execution of the CLA instruction. Repeat 11 more times, starting from each one of the register-reference instructions. the initial value of PC is hexadecimal 021.

### 3. 

The contents of PC in the basic computer is 3AF (all numbers in hexadecimal) the contents of AC is 7EC3 The contents of memory at address 3af is 932E the contents of memory at address 32E is 09AC The contents of memory at address 9AC is 8B9F

   a) What is the instruction that is fetched and executed next?
   
   b) Show the binary operation that will be performed in the AC when the instruction is executed.
   
   c) Give contents of registers PC, AR, DR, AC, and IR in hexadecimal and values of E, I, and the sequence counter SC in binary at the end of the instruction cycle.

### 4. 

A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. the instruction code format consists of six bits per the operation part and 14 bits per the address part (no indirect mode bit) two instruction are packed in one memory word, and a 40 – bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instruction in this computer.

## Unit – 2
1. Illustrate the characteristics of some common memory technologies.

2. What is the effect of executing the instruction? \texttt{MOV CX, [SOURCE_MEM]} 
   Where \texttt{SOURCE_MEM} equal to 2016 is a memory location offset relative to the current data segment starting at address 1A000\textsubscript{16}

3. The original contents of AX, BL, word-sized memory location SUM, and carry flag CF are 1234H, ABH, 00CDH, and 0H, respectively. Describe the results of executing the following sequence of instructions:

   \begin{align*}
   &\text{ADD AX, [SUM]} \\
   &\text{ADC BL, 05H} \\
   &\text{INC WORD PTR [SUM]}
   \end{align*}

4. Explain how different types of registers in 8086 microprocessor architecture are functioning compare among them?

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1. Illustrate the characteristics of some common memory technologies.

2. Compare and contrasts the micro programmed control and hard word wired unit

3. Show how the MRI And Non-MRI tables can be stored in memory

4. Obtain a flow chart for a program to check for a CR code (hexadecimal 0D) in a memory buffer. The buffer contains two characters per word. when the code for CR is encountered ,the program transfers it to bits 0 to 7 of location LNE without disturbing bits 8 through 15

---

1. Write your full name in ASCII using 8 bits per character with leftmost bit always 0. Include a space between names and a period after middle initial

2. Indicate whether the following constitute a control ,status, or data transfers commands
   a) Skip next instruction if flag is set
   b) Seek a given record on a magnetic disk
   c) Check if I/O device is ready
   d) Move printer paper to beginning of next page
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<th>Question</th>
<th>Answer</th>
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<tr>
<td>3. a) Synchronous serial communication</td>
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<tr>
<td>3. b) Asynchronous serial transmission with two stop bits</td>
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<tr>
<td>3. c) Asynchronous serial transmission with one stop bits</td>
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<tr>
<td>4. Why are the read and write control lines in a DMA controller bidirectional?</td>
<td>Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs?</td>
</tr>
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</table>

### Unit 5

1. Construct a diagram for 4x4 omega switching network. Show the switch setting required to connect input 3 to output 1.

2. Draw a diagram showing the structure of a four dimensional hypercube network. List all the paths available from node 7 to node 9 that use the minimum number of intermediate nodes.

3. Consider a bus topology in which two processors communicate through a buffer in shared memory. When one processor wishes to communicate with the other processor it puts the information in memory buffer and sets a flag. Periodically, the other processor checks the flags to determine if it has information to receive. What can be done to ensure proper synchronization and to minimize the time between sending and receiving the information?

4. The 8x8 omega switching network has three stages with four switches in each stage, for a total of 12 switches. How many stages and switches per stage are needed in an n x n omega switching network?

### Case Studies (With Higher Levels of thinking (Blooms Taxonomy))

**Note:** For every Case Study please mention the level of Blooms taxonomy

**1 (Covering Syllabus Up to Mid-1)**

1. The following control inputs are active in the bus system.

For each case, specify the register transfer that will be executed during the next clock transition.

<table>
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<tr>
<th>S2</th>
<th>s1</th>
<th>s0</th>
<th>LD of register</th>
<th>memory</th>
<th>Adder</th>
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<tbody>
<tr>
<td>a</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>IR</td>
<td>Read</td>
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2(Covering 2nd half of the Syllabus)

2. Consider a bus topology in which two processors communicate through a buffer in shared memory. When one processor wishes to communicate with the other processor it puts the information in the memory buffer and set a flag. Periodically, the other processor checks the flags to determine if it has information to receive. What can be done to ensure proper synchronization and to minimize the time between sending and receiving the information?

Unit Wise Multiple Choice Questions for CRT & Competitive Examinations

1. The decoded instruction is stored in ______ .
   a)IR
   b)PC
   c)Registers
   d) MDR

   Answer: a
   Explanation: The instruction after obtained from the PC, is decoded and operands are fetched and stored in the IR.

2. The instruction -> Add LOCA,R0 does,
   a) Adds the value of LOCA to R0 and stores in the temp register
   b) Adds the value of R0 to the address of LOCA
   c) Adds the values of both LOCA and R0 and stores it in R0
   d) Adds the value of LOCA with a value in accumulator and stores it in R0

   Answer: c
   Explanation: None
3. Which registers can interact with the secondary storage?
   a) MAR
   b) PC
   c) IR
   d) R0
   Answer: a
   Explanation: MAR can interact with secondary storage in order to fetch data from it.

4. During the execution of a program which gets initialized first?
   a) MDR
   b) IR
   c) PC
   d) MAR
   Answer: c
   Explanation: For the execution of a process first the instruction is placed in the PC.

5. Which of the register/s of the processor is/are connected to Memory Bus?
   a) PC
   b) MAR
   c) IR
   d) Both a and b.
   Answer: b
   Explanation: MAR is connected to the memory BUS in order to access the memory.

6. ISP stands for,
   a) Instruction Set Processor
   b) Information Standard Processing
   c) Interchange Standard Protocol
   d) Interrupt Service Procedure
   Answer: a
   Explanation: None.

7. The internal Components of the processor are connected by ________.
   a) Processor intra-connectivity circuitry
   b) Processor bus
c) Memory bus
d) Rambus

Answer: b
Explanation: The processor BUS is used to connect the various parts in order to provide a direct connection to the CPU.

8. ______ is used to choose between incrementing the PC or performing ALU operations.
   a) Conditional codes
   b) Multiplexer
   c) Control unit
   d) None of these

Answer: b
Explanation: The multiplexer circuit is used to choose between the two as it can give different results based on the input.

9. The registers, ALU and the interconnection between them are collectively called as _____ .
   a) Process route
   b) Information trail
   c) information path
   d) data path

Answer: d
Explanation: The Operational and processing part of the CPU are collectively called as data path.

10. This set of Computer Organization and Architecture MCQ focuses on “Different Addressing Modes of a System”.
11. The instruction, Add #45,R1 does,
    a) Adds the value of 45 to the address of R1 and stores 45 in that address
    b) Adds 45 to the value of R1 and stores it in R1
    c) Finds the memory location 45 and adds that content to that of R1
    d) None of the above

Answer: b
Explanation: The instruction is using immediate addressing mode hence the value is stored in the location 45 is added

12. In case of, Zero-address instruction method the operands are stored in _____ .
    a) Registers
b) Accumulators
c) Push down stack
d) Cache:

Answer: c
Explanation: In this case the operands are implicitly loaded onto the ALU

13. Add #45, when this instruction is executed the following happen/s,
   a) The processor raises an error and requests for one more operand
   b) The value stored in memory location 45 is retrieved and one more operand is requested
   c) The value 45 gets added to the value on the stack and is pushed onto the stack
   d) None of these
Answer: b
Explanation: None.

14. The addressing mode which makes use of in-direction pointers is _______.
   a) Indirect addressing mode
   b) Index addressing mode
   c) Relative addressing mode
   d) Offset addressing mode
Answer: a
Explanation: In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data

15. In the following indexed addressing mode instruction, MOV 5(R1),LOC the effective address is _______.
   a) EA = 5+R1
   b) EA = R1
   c) EA = [R1]
   d) EA = 5+[R1]
Answer: b
Explanation: In this the contents of the PC are directly incremented.

16. The addressing mode/s, which uses the PC instead of a general purpose register is _______.
   a) Indexed with offset
   b) Relative
   c) direct
   d) both a and c
Answer: d
Explanation: In case of, auto increment the increment is done afterwards and in auto decrement the decrement is done first.
17. When we use auto increment or auto decrement, which of the following is/are true
   1) In both, the address is used to retrieve the operand and then the address gets altered.
   2) In auto increment the operand is retrieved first and then the address altered.
   3) Both of them can be used on general purpose registers as well as memory locations.
      a) 1,2,3
      b) 2
      c) 1,3
      d) 2,3
      Answer: d
      Explanation: In case of, auto increment the increment is done afterwards and in auto decrement
      the decrement is done first.

18. The addressing mode, where you directly specify the operand value is _______.
      a) Immediate
      b) Direct
      c) Definite
      d) Relative
      Answer: a
      Explanation: None.

19. The effective address of the following instruction is , MUL 5(R1,R2)
      a) 5+R1+R2
      b) 5+(R1*R2)
      c) 5+[R1]+[R2]
      d) 5*([R1]+[R2])
      Answer: c
      Explanation: The addressing mode used is base with offset and index.

20. _____ addressing mode is most suitable to change the normal sequence of execution of
    instructions.
      a) Relative
      b) Indirect
      c) Index with Offset
      d) Immediate.
      Answer: a
      Explanation: The relative addressing mode is used for this since it directly updates the PC.
21. RTN stands for,
   a) Register Transfer Notation
   b) Register Transmission Notation
   c) Regular Transmission Notation
   d) Regular Transfer Notation
   Answer: a
   Explanation: This is the way of writing the assembly language code with the help of register notations.

22. The instruction, Add Loc,R1 in RTN is _______ .
   a) Add Set CC Loc+R1
   b) R1=Loc+R1
   c) Not possible to write in RTN
   d) R1<[Loc]+[R1] [expand title="View Answer"]
   Answer: d Explanation: None.

23. Can you perform addition on three operands simultaneously in ALN using Add instruction?
   a) Yes
   b) Not possible using Add, we’ve to use AddSetCC
   c) Not permitted
   d) None of the above
   Answer: c
   Explanation: You cannot perform addition on three operands simultaneously because the third operand is where the result is stored.

24. The instruction, Add R1,R2, R3 in RTN is _______ .
   a) R3=R1+R2+R3
   b) R3<-[R1]+[R2]+[R3] c) R3=[R1]+[R2] d) R3<-[R1]+[R2] [expand title="View Answer"]
   Answer: d Explanation: In RTN the first operand is the destination and the second operand is the source. [/expand]

25. In a system, which has 32 registers the register id is ____ long.
   a) 16 bits
   b) 8 bits
   c) 5 bits
   d) 6 bits
   Answer: c
   Explanation: The ID is the name tag given to each of the registers and used to identify them.
26. The two phases of executing an instruction are,
  a) Instruction decoding and storage
  b) Instruction fetch and instruction execution
  c) Instruction execution and storage
  d) Instruction fetch and Instruction processing

  Answer: d
  Explanation: The fetch ends with the instruction getting decoded and being placed in the IR and
  the PC getting incremented.

27. The Instruction fetch phase ends with,
  a) Placing the data from the address in MAR into MDR
  b) Placing the address of the data into MAR
  c) Completing the execution of the data and placing its storage address into MAR
  d) Decoding the data in MDR and placing it in IR

  Answer: d
  Explanation: The fetch ends with the instruction getting decoded and being placed in the IR and
  the PC getting incremented.

28. While using the iterative construct (Branching) in execution, ____ instruction is used to
   check the condition.
   a) TestAndSet
   b) Branch
   c) TestCondn
   d) None of the above

  Answer: b
  Explanation: Branch instruction is used to check the test condition and to perform the memory
  jump with help of offset.

29. When using Branching, the usual sequencing of the PC is altered. A new instruction is loaded
   which is called as ______ .
   a) Branch target
   b) Loop target
   c) Forward target
   d) Jump instruction

  Answer: a
  Explanation: None.

30. The condition flag Z is set to 1 to indicate,
   a) The operation has resulted in an error
   b) The operation requires an interrupt call
c) The result is zero

d) There is no empty register available

Answer: c

Explanation: This condition flag is used to check if the arithmetic operation yields a zero output

Unit-3

1. _____ converts the programs written in assembly language into machine instructions .
   a) Machine compiler
   b) Interpreter
   c) Assembler
   d) Converter
   Answer: c

   Explanation: The assembler is a software used to convert the programs into machine instructions

2. The instructions like MOV or ADD are called as ______ .
   a) OP-Code
   b) Operators
   c) Commands
   d) None of the above
   Answer: b

   Explanation: The ADDI instruction, means the addition is in immediate addressing mode.

3. The alternate way of writing the instruction, ADD #5,R1 is ______ .
   a) ADD [5],[R1];
   b) ADDI 5,R1;
   c) ADDIME 5,[R1];
   d) There is no other way
   Answer: b

   Explanation: The ADDI instruction, means the addition is in immediate addressing mode..

4. Instructions which won't appear in the object program are called as _____ .
   a) Redundant instructions
   b) Exceptions
   c) Comments
   d) Assembler Directives
   Answer: d
Explanation: The directives help the program in getting compiled and hence wont be there in the object code.

5. The assembler directive EQU, when used in the instruction : Sum EQU 200 does,
   a) Finds the first occurrence of Sum and assigns value 200 to it
   b) Replaces every occurrence of Sum with 200
   c) Re-assigns the address of Sum by adding 200 to its original address
   d) Assigns 200 bytes of memory starting the location of Sum
   Answer: b
   Explanation: This basically is used to replace the variable with a constant value.

6. The purpose of the ORIGIN directive is,
   a) To indicate the starting position in memory, where the program block is to be stored
   b) To indicate the starting of the computation code
   c) To indicate the purpose of the code
   d) To list the locations of all the registers used
   Answer: a
   Explanation: This does the function similar to the main statement..

7. The directive used to perform initialization before the execution of the code is ______ .
   a) Reserve
   b) Store
   c) Dataword
   d) EQU
   Answer: c
   Explanation: None..

8. _____ directive is used to specify and assign the memory required for the block of code .
   a) Allocate
   b) Assign
   c) Set
   d) Reserve
   Answer: d
   Explanation: This instruction is used to allocate a block of memory and to store the object code of the program there.

9. _____ directive specifies the end of execution of a program .
   a) End
   b) Return
   c) Stop
d) Terminate
Answer: b
Explanation: This instruction directive is used to terminate the program execution.

10. The last statement of the source program should be _______.
a) Stop
b) Return
c) OP
d) End
Answer: d
Explanation: This enables the processor to load some other process.

11. When dealing with the branching code the assembler,
a) Replaces the target with its address
b) Does not replace until the test condition is satisfied
c) Finds the Branch offset and replaces the Branch target with it
d) Replaces the target with the value specified by the DATAWORD directive
Answer: c
Explanation: When the assembler comes across the branch code, it immediately finds the branch offset and replaces it with it.

12. The assembler stores all the names and their corresponding values in _______.
a) Special purpose Register
b) Symbol Table
c) Value map Set
d) None of the above
Answer: b
Explanation: The table where the assembler stores the variable names along with their corresponding memory locations and values.

13. The assembler stores the object code in _______.
a) Main memory
b) Cache
c) RAM
d) Magnetic disk
Answer: d
Explanation: After compiling the object code, the assembler stores it in the magnetic disk and waits for further execution.

14. The utility program used to bring the object code into memory for execution is _______.
a) Loader
b) Fetcher

c) Extractor
d) Linker.

Answer: a
Explanation: The program which is used to load the program into memory.

15. To overcome the problems of the assembler in dealing with branching code we use _____ .
   a) Interpreter
   b) Debugger
   c) Op-Assembler
   d) Two-pass assembler

Answer: d
Explanation: This creates entries into the symbol table first and then creates the object code.

16. _______ are the different type/s of generating control signals.
   a) Micro-programmed
   b) Hardwired
   c) Micro-instruction
   d) Both a and b

Answer: d
Explanation: The above are used to generate control signals in different types of system architectures.

17. The type of control signal are generated based on,
   a) contents of the step counter
   b) Contents of IR
   c) Contents of condition flags
   d) All of the above

Answer: d
Explanation: Based on the information above the type of control signal is decided

18. What does the hardwired control generator consist of?
   a) Decoder/encoder
   b) Condition codes
   c) Control step counter
   d) All of the above
19. What does the end instruction do?
a) It ends the generation of a signal  
b) It ends the complete generation process  
c) It starts a new instruction fetch cycle and resets the counter  
d) It is used to shift the control to the processor  
Answer: c  
Explanation: It is basically used to start the generation of a new signal.

20. The Zin signal to the processor is generated using, \( Z_{in} = T_1 + T_6 \text{ ADD } + T_4 \) .  
a) True  
b) False  
Answer: a  
Explanation: The signal is generated using the logic of the formula above.

21. What does the RUN signal do?  
a) It causes the termination of a signal  
b) It causes a particular signal to perform its operation  
c) It causes a particular signal to end  
d) It increments the step counter by one  
Answer: d  
Explanation: The RUN signal increments the step counter by one for each clock cycle.

22. The name hardwired came because the sequence of operations carried out are determined by the wiring.  
a) True  
b) False  
Answer: a  
Explanation: In other words hardwired is another name for Hardware Control signal generator.

23. The benefit of using this approach is  
a) It is cost effective  
b) It is highly efficient  
c) It is very reliable
d) It increases the speed of operation
Answer: d
Explanation: <numeric> None.

24. The disadvantage/s of the hardwired approach is
a) It is less flexible
b) It cannot be used for complex instructions
c) It is costly
d) Both a and b
Answer: d
Explanation: <numeric> The more complex the instruction set less applicable is hardwired approach

25. The End signal is generated using, 
End = T7.ADD + T5.BR + (T5.N+ T4.-N).BRN…
a) True 
b) False
Answer: a
Explanation: <numeric> None.

26. In micro-programmed approach, the signals are generated by ______.
a) Machine instructions
b) System programs
c) Utility tools
d) None of the above
Answer: a
Explanation: <numeric> The machine instructions generate the signals.

27. A word whose individual bits represent a control signal is ______.
a) Command word
b) Control word
c) Co-ordination word
d) Generation word
Answer: b
Explanation: <numeric> The control word is used to get the different types of control signals required.

28. A sequence of control words corresponding to a control sequence is called ______.
a) Micro routine
b) Micro function

c) Micro procedure

d) None of the above

Answer: b

Explanation: <numeric> The control word is used to get the different types of control signals required

29. Individual control words of the micro routine are called as ______.

a) Micro task

b) Micro operation

c) Micro instruction

d) Micro command

Answer: c

Explanation: <numeric> The each instruction which put together performs the task.

30. The special memory used to store the micro routines of a computer is ________.

a) Control table

b) Control store

c) Control mart

d) Control shop

Answer: b

Explanation: <numeric> The control store is used as a reference to get the required control routine

31. To read the control words sequentially _________ is used.

a) PC

b) IR

c) UPC

d) None of the above

Answer: c

Explanation: <numeric> The UPC stands for Micro program counter.

32. Every time a new instruction is loaded into IR the output of _________ is loaded into UPC.

a) Starting address generator

b) Loader

c) Linker

d) Clock

Answer: a
Explanation: <numeric> The starting address generator is used to load the address of the next micro instruction.

33. The case/s where micro-programmed cannot perform well
   a) When it requires to check the condition codes
   b) When it has to choose between the two alternatives
   c) When it is triggered by an interrupt
   d) Both a and b
   Answer: d
   Explanation: <numeric> None.

34. The signals are grouped such that mutually exclusive signals are put together.
   a) True
   b) False
   Answer: a
   Explanation: <numeric> This is done to improve the efficiency of the controller.

35. Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is ________.
   a) Horizontal organization
   b) Vertical organization
   c) Diagonal organization
   d) None of the above
   Answer: b
   Explanation: <numeric> None.

Unit-4

1. The DMA differs from the interrupt mode by
   a) The involvement of the processor for the operation
   b) The method accessing the I/O devices
   c) The amount of data transfer possible
   d) Both a and c
   Answer: d
   Explanation: DMA is an approach of performing data transfers in bulk between memory and the external device without the intervention of the processor.

2. The DMA transfers are performed by a control circuit called as
   a) Device interface
   b) DMA controller
c) Data controller
d) overlooker
Answer: b
Explanation: The Controller performs the functions that would normally be carried out by the processor.

3. In DMA transfers, the required signals and addresses are given by the
   a) Processor
   b) Device drivers
   c) DMA controllers
   d) The program itself
   Answer: c
   Explanation: The DMA controller acts like a processor for DMA transfers and overlooks the entire process.

4. After the completion of the DMA transfer the processor is notified by
   a) Acknowledge signal
   b) Interrupt signal
   c) WMFC signal
   d) None of the above
   Answer: b
   Explanation: The controller raises an interrupt signal to notify the processor that the transfer was complete.

5. The DMA controller has ______ registers
   a) 4
   b) 2
   c) 3
   d) 1
   Answer: a
   Explanation: None.

6. When the R/W bit of the status register of the DMA controller is set to 1,
   a) Read operation is performed
   b) Write operation is performed
   Answer: b
   Explanation: The controller is directly connected to the system BUS to provide faster transfer of data.

7. The controller is connected to the ______
   a) Processor BUS
b) System BUS  
c) External BUS  
d) None of the above  
Answer: b  
Explanation: The controller is directly connected to the system BUS to provide faster transfer of data.

8. Can a single DMA controller perform operations on two different disks simultaneously...??  
a) True  
b) False  
Answer: a  
Explanation: The DMA controller can perform operations on two different disks if the appropriate details are known.

9. The technique where the controller is given complete access to main memory is  
a) Cycle stealing  
b) Memory stealing  
c) Memory Con  
d) Burst mode  
Answer: c  
Explanation: The controller takes over the processor’s access cycles and performs memory operations.

Explanation: The controller is given full control of the memory access cycles and can transfer blocks at a faster rate.

10. The controller uses _____ to help with the transfers when handling network interfaces.  
a) Input Buffer storage  
b) Signal enhancers  
c) Bridge circuits  
d) All of the above  
Answer: a  
Explanation: The controller stores the data to transferred in the buffer and then transfers it.

11. To overcome the conflict over the possession of the BUS we use ______  
a) Optimizers  
b) BUS arbitrators  
c) Multiple BUS structure  
d) None of the above  
Answer: b  
Explanation: The BUS arbitrator is used overcome the contention over the BUS possession.
12. The registers of the controller are ______
a) 64 bits  
b) 24 bits  
c) 32 bits  
d) 16 bits  
Answer: c  
Explanation: None

13. When process requests for a DMA transfer ,
a) Then the process is temporarily suspended  
b) The process continues execution  
c) Another process gets executed  
d) Both a and c  
Answer: d  
Explanation: The process requesting the transfer is paused and the operation is performed , meanwhile another process is run on the processor.

14. The DMA transfer is initiated by _____
a) Processor  
b) The process being executed  
c) I/O devices  
d) OS  
Answer: c  
Explanation: The transfer can only be initiated by instruction of a program being executed.

15. In memory-mapped I/O…
a) The I/O devices and the memory share the same address space  
b) The I/O devices have a separate address space  
c) The memory and I/O devices have an associated address space  
d) A part of the memory is specifically set aside for the I/O operation  
Answer: a  
Explanation: Its the different modes of accessing the i/o devices.

16. The usual BUS structure used to connect the I/O devices is
a) Star BUS structure  
b) Multiple BUS structure  
c) Single BUS structure  
d) Node to Node BUS structure
Answer: c
Explanation: BUS is a collection of address, control and data lines used to connect the various devices of the computer

17. In Intel’s IA-32 architecture there is a separate 16 bit address space for the I/O devices??
   a) False
   b) True
Answer: b
Explanation: This type of accessing is called as I/O mapped devices.

18. The advantage of I/O mapped devices to memory mapped is
   a) The former offers faster transfer of data
   b) The devices connected using I/O mapping have a bigger buffer space
   c) The devices have to deal with fewer address lines
   d) No advantage as such
Answer: c
Explanation: Since the I/O mapped devices have a separate address space the address lines are limited by amount of the space allocated.

19. The system is notified of a read or write operation by
   a) Appending an extra bit of the address
   b) Enabling the read or write bits of the devices
   c) Raising an appropriate interrupt signal
   d) Sending a special signal along the BUS
Answer: d
Explanation: It is necessary for the processor to send a signal intimating the request as either read or write.

20. To overcome the lag in the operating speeds of the I/O device and the processor we use
   a) Buffer spaces
   b) Status flags
   c) Interrupt signals
   d) Exceptions
Answer: b
Explanation: The processor operating is much faster than that of the I/O devices, so by using the status flags the processor need not wait till the I/O operation is done. It can continue with its work until the status flag is set.
21. The method of accessing the I/O devices by repeatedly checking the status flags is
   a) Program-controlled I/O
   b) Memory-mapped I/O
   c) I/O mapped
   d) None
   Answer: a
   Explanation: In this method the processor constantly checks the status flags, and when it finds that the flag is set it performs the appropriate operation.

22. The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is
   a) Exceptions
   b) Signal handling
   c) Interrupts
   d) DMA
   Answer: c
   Explanation: This is a method of accessing the I/O devices which gives the complete power to the devices, enabling them to intimate the processor when they’re ready for transfer.

23. Which offers higher speeds of I/O transfers is
   a) Interrupts
   b) Memory mapping
   c) Program-controlled I/O
   d) DMA
   Answer: d
   Explanation: In DMA the I/O devices are directly allowed to interact with the memory without the intervention of the processor and the transfers take place in the form of blocks increasing the speed of operation.

24. The process where in the processor constantly checks the status flags is called as
   a) Polling
   b) Inspection
   c) Reviewing
   d) Echoing
   Answer: a
   Explanation: None.
Unit-5

1. A single machine instruction can controls the simultaneous execution of a number of processing elements on

   A. Lockstep Basis  
   B. Open Step Basis  
   C. Early Basis  
   D. None

   Answer A

2. A sequence of data is transmitted to a set of

   A. Devices  
   B. Resources  
   C. Computers  
   D. Processors

   Answer D

3. A set of processors simultaneously execute different instructions sequence on different

   A. Buffers  
   B. Data Set  
   C. Buses  
   D. Registers

4. A single processor executes a single instruction stream to operate on data stored in a single

   A. Computer  
   B. System  
   C. Memory  
   D. Device

   Answer C

5. The design of SMPs and Cluster is

   A. Same  
   B. Different
C. Complex
D. Easy

6. Symmetric multiprocessing in the computer system does not use

A. master relationship
B. slave relationship
C. master slave relationship
D. serial processing

Answer C

7. Multiprocessing provided by the computer system is of the type

A. symmetric multiprocessor
B. asymmetric multiprocessing
C. symmetric multiprocessing
D. both b and c

Answer D

8. SMP of the computer system is an abbreviation of

A. symmetric multiprocessor
B. asymmetric multiprocessor
C. symmetric multiprocessing
D. asymmetric multiprocessing

Answer D

9. Asymmetric multiprocessing systems of the computer system use

A. master relationship
B. slave relationship
C. master slave relationship
D. serial processing

Answer C

10. In symmetric multiprocessing of the computer system all processors are
A. peers
B. parallel
C. master slave
D. serial

Answer A

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