ACADEMIC REGULATIONS, COURSE STRUCTURE
AND DETAILED SYLLABUS

M.Tech (EMBEDDED SYSTEMS)

FOR
MASTER OF TECHNOLOGY TWO YEAR POST GRADUATE COURSE
(Applicable for the batches admitted from 2014-2015)

R14

ANURAG
Engineering Engineers

ANURAG GROUP OF INSTITUTIONS
(AUTONOMOUS)
SCHOOL OF ENGINEERING
Venkatapur, Ghatkesar, Hyderabad – 500088
## ANURAG GROUP OF INSTITUTIONS
(AUTONOMOUS)

### M.TECH (EMBEDDED SYSTEMS)

#### COURSE STRUCTURE AND SYLLABUS

### I Year I Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>P</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td>A31065</td>
<td>Embedded System Design</td>
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<td>0</td>
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<tr>
<td>A31066</td>
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<td>A31067</td>
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<tr>
<td>A31068</td>
<td>Embedded C</td>
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<tr>
<td><strong>Elective-I</strong></td>
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<tr>
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<td>Advanced Computer Architecture</td>
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<tr>
<td>A31070</td>
<td>VLSI Technology and Design</td>
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<tr>
<td>A31071</td>
<td>Embedded Computing</td>
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<td><strong>Elective-II</strong></td>
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<tr>
<td>A31072</td>
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<td>A31073</td>
<td>Soft Computing Techniques</td>
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### I Year II Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
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<tbody>
<tr>
<td>A32067</td>
<td>Hardware Software Co-Design</td>
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</tr>
<tr>
<td>A32068</td>
<td>Digital Signal Processors And Architectures</td>
<td>3</td>
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<td>A32069</td>
<td>Embedded Networking</td>
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<td>0</td>
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<td>A32070</td>
<td>CPLD and FPGA Architectures and Applications</td>
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<td>A32071</td>
<td>Sensors and Actuators</td>
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<td>A32072</td>
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<td>A32073</td>
<td>Network Security and Cryptography</td>
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<td>A32074</td>
<td>Multimedia and Signal Coding</td>
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<tr>
<td>A32075</td>
<td>System On Chip Architecture</td>
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<td>A32076</td>
<td>Wireless LANs and PANs</td>
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<td>A32215</td>
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<td>A32216</td>
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### II YEAR I SEMESTER

<table>
<thead>
<tr>
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<th>Subject Name</th>
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<th>Credits</th>
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<tr>
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<td>Comprehensive Viva</td>
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<td>-</td>
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</tr>
<tr>
<td>A33223</td>
<td>Project Seminar - I</td>
<td></td>
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<tr>
<td>A33224</td>
<td>Project Work</td>
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<td><strong>Total Credits</strong></td>
<td></td>
<td></td>
<td><strong>22</strong></td>
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### II YEAR II SEMESTER

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject Name</th>
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<th>Credits</th>
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<td>Project Work and Seminar</td>
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<tr>
<td></td>
<td><strong>Total Credits</strong></td>
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<td></td>
<td><strong>22</strong></td>
</tr>
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</table>
Academic Regulations for M. Tech (Regular) Degree Course
(Effective for the students admitted into I year from the Academic Year 2014-2015 onwards)

The M.Tech Degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the program and fulfill all the requirements for the award of the degree.

1.0 ELIGIBILITY FOR ADMISSIONS:
Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by the university from time to time.

Admissions shall be made on the basis of merit rank obtained by the qualifying candidate at an Entrance Test conducted by the University or on the basis of any other order of merit approved by the University, subject to reservations prescribed by the university from time to time.

2.0 AWARD OF M.TECH DEGREE:
2.1 A student shall be declared eligible for the award of the M.Tech degree, if he pursues a course of study and completes it successfully for not less than two academic years and not more than four academic years.

2.2 A Student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his admission, shall forfeit his seat in M.Tech course.

2.3 The minimum instruction period for each semester is 90 clear instruction days.

3.0 COURSE OF STUDY
The following specializations are offered at present for the M.Tech Course of study.

1. CAD / CAM
2. Computer Science
3. Computer Science and Engineering
4. Electrical Power systems
5. Electronics and Communication Engineering
6. Embedded Systems
7. Machine Design
8. Power Electronics and Electrical Drives
9. Software Engineering
10. Structural Engineering
11. VLSI System Design
12. Wireless and Mobile Communications
13. Computer Networks and Information Security
14. Construction Management
4.0 ATTENDANCE:

The programs are offered on unit basis with each subject being considered as an unit.
4.1 A candidate shall be deemed to have eligibility to write end semester examinations in a
subject if he has put in at least 75% of attendance in the subject.
4.2 Shortage of attendance up to 10% in any subject (i.e. 65% and above and below 75%)
may be condoned by the college Academic council on genuine and valid reasons on
representation by the candidate with supporting evidence.
4.3 A candidate shall get minimum required attendance at least in three (3) theory subjects in
the present semester to get promoted to the next semester. In order to qualify for the
award of the M.Tech Degree, The candidate shall complete all the academic
requirements of the subjects, as per the course structure.
4.4 Shortage of attendance below 65% shall in no case be condoned
4.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

5.0 EVALUATION:

The performance of the candidate in each semester shall be evaluated subject-wise, with a
maximum of 100 marks for theory and 100 marks for practicals, on the basis of internal evaluation
and End semester Examination.

For the theory subjects 60 marks shall be awarded based on the performance in the End semester
Examination, 30 marks shall be awarded based on the internal evaluation and 10 marks for
assignment.

5.1 For theory subjects, during the semester there shall be 2 midterm examinations. Each
midterm examination consists of one subjective paper and one assignment. The subjective
paper is for 30 marks with duration of 2 hours. Subjective paper of each semester shall
contain 2 parts Section-A & Section-B. Section-A comprises of five (5) short answer type
of questions. The student has to answer all the questions from section-A. Each question
carries two marks. A total of ten marks are allocated to section-A. Section-B consists of
five (5) essay type of questions from which the student has to answer three questions.
Each question carry not more than seven (7) marks. A total of 20 marks are allocated for
section-B. The questions in the first midterm examination includes the topics of first 2.5
units while the questions in the second midterm examination includes the topics of
remaining 2.5 units. The assignments should be submitted before the conduct of respective
midterm examinations.

The total marks secured by the student are out of 40 marks (30marks from midterm
examination and 10 marks from assignment) in an internal examination for a subject. The
average of marks secured in two midterm examinations shall be taken as final marks. If
he/she is absent for any test / assignment, he/she are awarded zero marks for that test /
assignment.

5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End
Semester Examinations, 40 marks shall be awarded based on the day-to-day performance
as internal marks.

5.3 There shall be two seminar presentations during I year I semester and II Semester. For
seminar, a student under the supervision of a faculty member, shall collect the literature on
a topic and critically review the literature and submit it to the department in a report from and shall make an oral presentation before the departmental committee. The departmental committee consists of Head of the department, supervisor and two other senior faculty members of the department. For each seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful.

5.4 There shall be a Comprehensive Viva-Voce in II year I Semester. The comprehensive Viva-Voce will be conducted by a committee consisting of Head of the Department and two Senior Faculty members of the Department. The comprehensive Viva-Voce is aimed to assess the students' understanding in various subjects he/she studies during the M.Tech course of study. The Comprehensive viva-voce valued for 100 marks by the Committee. There are no internal marks for the Comprehensive viva-Voce.

5.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 4.3) he has to reappear for the End Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and he has failed in the end examination. In such case candidate must re-register subject(s) and secure required minimum attendance. Attendance in the re-registered subject(s) has to be calculated separately to become eligible to write the end examination in the re-registered subject(s). The attendance of re-registered subject(s) shall be calculated separately to decide upon the eligibility for writing the end examination in those subject(s). In the event of taking another chance, the internal marks and end examination marks obtained in the previous attempt are nullified.

5.7 In case the candidate secures less than the required attendance in any subject(s), he shall not be permitted to appear for the End Examination in that subject(s). He shall re-register the subject when next offered.

5.8 Laboratory examination for M.Tech courses must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be other Laboratory Teacher.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the project review committee.

6.1 A Project Review Committee (PRC) shall be constituted with Principal as chair person, Heads of all the departments which are offering the M.Tech programs and two other senior faculty members.

6.2 Registration of Project work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical subjects).

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the Departmental
Committee for its approval. Only after obtaining the approval of Departmental Committee the student can initiate the Project work.

6.4 If a candidate wishes to change his supervisor or topic of the project he can do so with the approval of Departmental Committee. However, the Departmental Committee shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.5 A candidate shall submit status report (in a bound-form) in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters. A candidate is permitted to submit project thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal (through Head of the Department) and shall make an oral presentation before the PRC.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the Institution. For this, Chairman, BOS of the respective departments shall submit a panel of 5 examiners, who are eminent in that field with the help of the concerned guide and senior faculty of the department.

6.9 If the report of the examiner is not favourable, the candidate shall revise and resubmit the thesis, in the time frame as prescribed by PRC. If the report of the examiner is unfavourable again the thesis shall be summarily rejected.

6.10 If the report of the examiner is favourable, viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner who adjudicated the Thesis.

The Board shall jointly report candidates work as:

A. EXCELLENT
B. GOOD
C. SATISFACTORY
D. UNSATISFACTORY

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination. If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, he will not be eligible for the award of the degree.
7.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirement prescribed for the completion of the program and is eligible for the award of M.Tech Degree, he shall be placed in one of the following four classes.

<table>
<thead>
<tr>
<th>Classes Awarded</th>
<th>% of marks to be secured</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Class with Distinction</td>
<td>70% and above</td>
</tr>
<tr>
<td>First Class</td>
<td>Below 70% but not less than 60%</td>
</tr>
<tr>
<td>Second Class</td>
<td>Below 60% but not less than 50%</td>
</tr>
</tbody>
</table>

(The marks in internal evaluation and end examination shall be shown separately in the marks memorandum)

8.0 WITHHOLDING OF RESULTS:

If the candidate has not paid any dues to the institution or if any case of in-discipline is pending against him, the result of the candidate will be withheld and he will not be allowed into next higher semester. The issue of the degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS:

Candidate who have discontinued or have been detained for want of attendance or who have failed after having undergone the course are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to 5.5 and 2.0

10.0 GENERAL:

10.1 The academic regulations should be read as a whole for purpose of any interpretation.
10.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.
10.3 The institution may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the institution.
10.4 Wherever the word he, him or his occur, it will also include she, her and hers. There shall be no transfers within the constituent colleges of Jawaharlal Nehru Technological University.
# MALPRACTICES RULES

## DISCIPLINARY ACTION FOR IMPROPER CONDUCT IN EXAMINATIONS

<table>
<thead>
<tr>
<th>Nature of Malpractices/Improper conduct</th>
<th>Punishment</th>
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</thead>
<tbody>
<tr>
<td>If the candidate:</td>
<td></td>
</tr>
<tr>
<td>1. (a) Possesses of keeps accessible in examination hall, any paper, note book, programmable calculators, cell phones, pager, palm, computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject only</td>
</tr>
<tr>
<td>(b) Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.</td>
</tr>
<tr>
<td>2. Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The hall ticket of the candidate is to be cancelled and sent to the controller of examinations, AGI.</td>
</tr>
<tr>
<td>3. Impersonates any other candidate in connection with the examination.</td>
<td>The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination(including practical’s and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.</td>
</tr>
<tr>
<td>4. Smuggles in the Answer book or</td>
<td>Expulsion from the examination hall and</td>
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<tr>
<td>5.</td>
<td>Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.</td>
</tr>
<tr>
<td>6.</td>
<td>Refuses to obey the orders of the Chief Superintendent/Assistant-Superintendent/any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any office relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.</td>
</tr>
<tr>
<td>7.</td>
<td>Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.</td>
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<tr>
<td></td>
<td>Posses any lethal weapon or firearm in the examination hall.</td>
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</tr>
<tr>
<td>9.</td>
<td>If student of the college, who is not a candidate for the particular examination or any person not connected with college indulges in any malpractice or improper conduct mentioned in clause 6 to 8</td>
</tr>
<tr>
<td>10.</td>
<td>Comes in a drunken condition to the examination hall.</td>
</tr>
<tr>
<td>11.</td>
<td>Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.</td>
</tr>
<tr>
<td>12.</td>
<td>If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Malpractices committee, AGI for further action to award suitable punishment.</td>
</tr>
</tbody>
</table>
UNIT I:
Introduction to Embedded Systems

UNIT II:
Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT III:
Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT IV:
RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT V:
Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:
1. Embedded Systems - Raj Kamal, TMH.
4. An Embedded Software Primer - David E. Simon, Pearson Education.
M.TECH. (EMBEDDED SYSTEMS)-R13 Regulations

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech – 1 Year – 1 Sem. Embedded Systems

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT –I:
ARM Architecture:
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:
ARM Programming Model – I:
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:
ARM Programming Model – II:
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:
ARM Programming:
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:
Memory Management:

TEXT BOOKS:

REFERENCE BOOKS:
M.TECH. (EMBEDDED SYSTEMS)-R13 Regulations

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT - I:
Introduction
Introduction to UNIX/Linux, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II:
Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency, Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:
Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clock, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations

UNIT - V:
Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:

REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh
M.TECH (EMBEDDED SYSTEMS) - R13 Regulations

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech - I Year - I Sem. Embedded Systems

EMBEDDED C

UNIT – I:
Programming Embedded Systems in C
Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions
Introducing the 8051 Microcontroller Family
Introduction, What’s in a name, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions

UNIT – II:
Reading Switches
Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goots, Conclusions

UNIT – III:
Adding Structure to the Code
Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the ‘Hello Embedded World’ example, Example: Restructuring the goot-counting example, Further examples, Conclusions

UNIT – IV:
Meeting Real-Time Constraints
Introduction, Creating ‘hardware delays’ using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for ‘timeout’ mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V:
Case Study: Intruder Alarm System
Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

REFERENCE BOOKS:
1. PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner
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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE -I)

UNIT -I:
Fundamentals of Computer Design:
Fundamentals of computer design. Changing faces of computing and task of computer designer.
Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative
principles of computer design, Amdahl’s law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-
type and size of operands, Operations in the instruction set.

UNIT –II:
Pipelines:
Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five
stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing
pipeline branch penalties.
Memory Hierarchy Design:
Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual
memory.

UNIT –III:
Instruction Level Parallelism (ILP) - The Hardware Approach:
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach,
Branch prediction, High performance instruction delivery- Hardware based speculation.
ILP Software Approach:
Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism
at compile time, Cross cutting issues - Hardware versus Software.

UNIT –IV:
Multi Processors and Thread Level Parallelism:
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain,
Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V:
Inter Connection and Networks:
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples
of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

REFERENCE BOOKS:
   Scalar Processors
VLSI TECHNOLOGY AND DESIGN
(ELECTIVE -I)

UNIT -I:
Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BICMOS Technology.

Basic Electrical Properties of MOS, CMOS & BICMOS Circuits: \( I_{ch} - V_{th} \) relationships, Threshold Voltage \( V_{th} \), \( G_{ds} \), \( G_{ds} \) and \( \omega_{n} \). Pass Transistor, MOS, CMOS & Bi CMOS Inverters, \( Z_{in}, I_{in} \), MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT -II:
Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT -III:
Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT -IV:
Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT -V:
Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

REFERENCE BOOKS:
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EMBEDDED COMPUTING
(ELECTIVE – I)

UNIT -I:
Programming on Linux Platform:

UNIT -II:
Introduction to Software Development Tools:
GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

UNIT -III:
Interfacing Modules:
Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT -IV:
Networking Basics:
Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT -V:
IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS:
2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens
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DIGITAL SYSTEM DESIGN
(ELECTIVE -II)

UNIT -I:
Minimization and Transformation of Sequential Machines:
The Finite State Model -- Capabilities and limitations of FSM -- State equivalence and machine
minimization -- Simplification of incompletely specified machines.
Fundamental mode model -- Flow table -- State reduction -- Minimal closed covers -- Races, Cycles
and Hazards.

UNIT -II:
Digital Design:
Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 -- bit adder, State graphs for control
circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner,
Binary divider.

UNIT -III:
SM Charts:
State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary
Multiplier, dice game controller.

UNIT -IV:
Fault Modeling & Test Pattern Generation:
Logic Fault model -- Fault detection & Redundancy- Fault equivalence and fault location --Fault
dominance -- Single stuck at fault model -- Multiple stuck at fault models --Bridging fault model.
Fault diagnosis of combinational circuits by conventional methods -- Path sensitization techniques,
Boolean Difference method -- Kohavi algorithm -- Test algorithms -- D algorithm, PODEM, Random
testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:
Fault Diagnosis in Sequential Circuits:
Circuit Test Approach, Transition Check Approach -- State identification and fault detection
experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:
2. Digital Systems Testing and Testable Design -- Miron Abramovici, Melvin A.
   Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory -- N. N. Biswas, PHI

REFERENCE BOOKS:
3. Digital Circuits and Logic Design -- Samuel C. Lee, PHI
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SOFT COMPUTING TECHNIQUES
(ELECTIVE -II)

UNIT -I:
Introduction:
Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT -II:
Artificial Neural Networks:
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT -III:
Fuzzy Logic System:
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT -IV:
Genetic Algorithm:
Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and Ant-colony search techniques for solving optimization problems.

UNIT -V:
Applications:

TEXT BOOKS:

REFERENCE BOOKS:
6. Artificial Neural Network -Simon Haykin, 2nd Ed., Pearson Education.
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ADVANCED OPERATING SYSTEMS
(ELECTIVE -II)

UNIT –I:
Introduction to Operating Systems:
Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:
Introduction to UNIX and LINUX:
Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations

UNIT –III:
System Calls:
System calls and related file structures, Input / Output, Process creation & termination.
Inter Process Communication
Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:
Introduction to Distributed Systems:
Goals of distributed system, Hardware and software concepts, Design issues.
Communication in Distributed Systems:
Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:
Synchronization in Distributed Systems:
Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions
Deadlocks:
Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:
1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.

REFERENCE BOOKS:
M.TECH. (EMBEDDED SYSTEMS)-R13 Regulations

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EMBEDDED C LABORATORY

Note:

- Minimum of 10 experiments have to be conducted.
- The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 ms delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions.
11. Program to Sort RTOS on to 89C51 development board.
12. Program to Interface Elevator.
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HARDWARE - SOFTWARE CO-DESIGN

UNIT -I:
Co- Design Issues:
Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co- Synthesis Algorithms:
Hardware software synthesis algorithms: hardware -- software partitioning distributed system co-
synthesis.

UNIT -II:
Prototyping and Emulation:
Prototyping and emulation techniques, prototyping and emulation environments, future developments
in emulation and prototyping architecture specialization techniques, system communication
infrastructure

Target Architectures:
Architecture specialization techniques, System Communication infrastructure, Target Architecture
and Application System classes, Architecture for control dominated systems (8051-Architectures for
High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60),
Mixed Systems.

UNIT -III:
Compilation Techniques and Tools for Embedded Processor Architectures:
Modern embedded architectures, embedded software development needs, compilation technologies,
practical consideration in a compiler development environment.

UNIT -IV:
Design Specification and Verification:
Design, co-design, the co-design computational model, concurrency coordinating concurrent
computations, interfacing components, design verification, implementation verification, verification
tools, interface verification

UNIT -V:
Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level
specification languages.
Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos
system.

TEXT BOOKS:
2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer
Academic Publishers

REFERENCE BOOKS:
1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer
UNIT I:
Introduction to Digital Signal Processing:
Introduction, a digital signal-processing system, the sampling process, discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.
Computational Accuracy in DSP Implementations:
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II:
Architectures for Programmable DSP Devices:
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

UNIT III:
Programmable Digital Signal Processors:
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT IV:
Analog Devices Family of DSP Devices:
Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT V:
Interfacing Memory and I/O Peripherals to Programmable DSP Devices:
Memory space organization, External bus interfacing signals, Memory Interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

REFERENCE BOOKS:
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
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EMBEDDED NETWORKING

UNIT -I:
Embedded Communication Protocols:

UNIT -II:
USB and CAN Bus:
USB bus - Introduction - Speed Identification on the bus - USB States - USB bus communication; Packets - Data flow types - Enumeration - Descriptors - PIC 18 Microcontroller USB Interface - C Programs - CAN Bus - Introduction - Frames - Bit stuffing - Types of errors - Nominal Bit Timing - PIC microcontroller CAN Interface - A simple application with CAN.

UNIT -III:
Ethernet Basics:

UNIT -IV:
Embedded Ethernet:
Exchanging messages using UDP and TCP - Serving web pages with Dynamic Data - Serving web pages that respond to user input - Email for Embedded Systems - Using FTP - Keeping Devices and Network secure.

UNIT -V:
Wireless Embedded Networking:

TEXT BOOKS:

REFERENCE BOOKS:
1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
UNIT-I:
Introduction to Programmable Logic Devices:
Introduction, Simple Programmable Logic Devices - Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices - Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II:
Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT-III:
SRAM Programmable FPGAs:

UNIT -IV:
Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:
Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

REFERENCE BOOKS:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
3. Digital Systems Design with FPGAs and CPLDs - Ian Groul, Elsevier, Newnes.
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SENSORS AND ACTUATORS
(ELECTIVE -III)

UNIT I:
Sensors / Transducers: Principles -- Classification -- Parameters -- Characteristics - Environmental Parameters (EP) -- Characterization

UNIT II:

UNIT III:
Radiation Sensors: Introduction -- Basic Characteristics -- Types of Photosensors/Photo detectors -- X-ray and Nuclear Radiation Sensors -- Fiber Optic Sensors

UNIT IV:
Smart Sensors: Introduction -- Primary Sensors -- Excitation -- Amplification -- Filters -- Converters -- Compensation -- Information Coding/Processing -- Data Communication -- Standards for Smart Sensor Interface -- The Automation

UNIT V:
Actuators: Pneumatic and Hydraulic Actuation Systems -- Actuation systems -- Pneumatic and hydraulic systems -- Directional Control valves -- Pressure control valves -- Cylinders -- Servo and proportional control valves -- Process control valves -- Rotary actuators
Mechanical Actuation Systems -- Types of motion -- Kinematic chains -- Cams -- Gears -- Ratchet and pawl -- Belt and chain drives -- Bearings -- Mechanical aspects of motor selection
Electrical Actuation Systems -- Electrical systems -- Mechanical switches -- Solid-state switches -- Solenoids -- D.C. Motors -- A.C. motors -- Stepper motors

TEXT BOOKS:

REFERENCE BOOKS:
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WIRELESS COMMUNICATIONS AND NETWORKS
(ELECTIVE -III)

UNIT -I:

UNIT -II:

UNIT -III:
Mobile Radio Propagation: Small -Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke’s model for flat fading, spectral shape due to Doppler spread in Clarke’s model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT -IV:

UNIT -V:
Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparison of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.

TEXT BOOKS:

REFERENCE BOOKS:
2. Wireless Digital Communications – Kemilo Fehrer, 1999, PHI.
NETWORK SECURITY AND CRYPTOGRAPHY
(ELECTIVE - III)

UNIT – I:
Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A
Model for network security. Classical Techniques: Conventional Encryption model,
Steganography, Classical Encryption Techniques.

UNIT – II:
Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard,
Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of
operations. Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2,
Characteristics of Advanced Symmetric block ciphers. Conventional Encryption: Placement of Encryption function,
Traffic confidentiality, Key distribution, Random Number Generation. Public Key Cryptography: Principles, RSA Algorithm,
Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT – III:
Number Theory: Prime and relatively prime numbers, Modular arithmetic, Fermat's and Euler's
theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete
logarithms. Message authentication and Hash Functions: Authentication requirements and functions,
Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT – IV:
Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPERM-160, HMAC.
Digital signatures and Authentication Protocols: Digital signatures, Authentication
Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT – V:
security Associations, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security,
Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:
   Education.
   Education.

REFERENCE BOOKS:
1. Fundamentals of Network Security by Eric Maivald (Dreamtech press)
   Perlman and Mike Speciner, Pearson/PHI.
5. Introduction to Cryptography, Buchmann, Springer.
UNIT I:


UNIT II:
Audio Concepts: Digitization of Sound, Quantization and Transmission of Audio.

UNIT III:
Compression Algorithms:
Lossless Compression Algorithms: Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.
Lossy Image Compression Algorithms: Transform Coding: KLT And DCT Coding, Wavelet Based Coding.

UNIT IV:
Video Compression Techniques: Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT V:

TEXT BOOKS:

REFERENCE BOOKS:
5. Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002
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SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

UNIT -I:
Introduction to the System Approach:
System Architecture, Components of the system, Hardware & Software, Processor Architectures,
Memory and Addressing, System level interconnection, An approach for SOC Design, System
Architecture and Complexity.

UNIT -II:
Processors:
Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts
in Processor Micro Architecture, Basic elements in Instruction handling, Buffers: minimizing Pipeline
Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions,
VLIW Processors, Superscalar Processors.

UNIT -III:
Memory Design for SOC:
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache
Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of
Cache, Split - I, and D - Caches, Multilevel Caches, Virtual to real translation , SOC Memory
System, Models of Simple Processor – memory interaction.

UNIT -IV:
Interconnect Customization and Configuration:
Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models,
Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An
overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto
Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -
overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT -V:
Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG
compression.

TEXT BOOKS:
1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India
   Pvt. Ltd.
   Professional.

REFERENCE BOOKS:
1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004,
   Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded
   Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter
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WIRELESS LANS AND PANS
(ELECTIVE-IV)

UNIT -I:
Wireless System & Random Access Protocols:

UNIT -II:
Wireless LANs:

UNIT -III:
The IEEE 802.11 Standard for Wireless LANs:

UNIT -IV:
Wireless PANs:
Introduction, Importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth Interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scalable network formation.

UNIT -V:
The IEEE 802.15 working Group for WPANs:
The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.

TEXT BOOKS:

REFERENCE BOOKS:
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EMBEDDED SYSTEMS LABORATORY

Note:
A. The following programs are to be implemented on ARM based Processors/Equivalent.
B. Minimum of 10 programs from Part --I and 6 programs from Part --II are to be conducted.

PART - I:
The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication | Division
   b. Operating Modes, System Calls and Interrupts
   c. Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

PART - II:
Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs (Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
   b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

Interfacing Programs:
6. Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.