ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABUS

R15

M.Tech (EMBEDDED SYSTEMS)

FOR
MASTER OF TECHNOLOGY TWO YEAR POST GRADUATE COURSE
(Applicable for the batches admitted from 2015-2016)

ANURAG GROUP OF INSTITUTIONS
(AUTONOMOUS)
Venkatapur, Ghatkesar, Hyderabad – 501301
Applicable for the students of M. Tech. (Regular) programme from the Academic Year 2015-16 and onwards

The M. Tech. Degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the programme and who fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.0 AWARD OF M. TECH. DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years, failing which he shall forfeit his seat in M. Tech. programme.

2.2 The student shall register for all 88 credits and secure all the 88 credits.

2.3 The minimum instruction days in each semester are 90.

3.0 COURSES OF STUDY

The following specializations are offered at present for the M. Tech. programme of study.

1. CAD/CAM
2. Computer Networks and Information Security
3. Computer Science
4. Computer Science and Engineering
5. Construction Management
6. Electrical Power Systems
7. Electronics and Communication Engineering
8. Embedded Systems
9. Machine Design
10. Power Electronics and Electrical Drives
11. Software Engineering
12. Structural Engineering
13. VLSI System Design
14. Wireless and Mobile Communication
Course Registration

4.1 A ‘Faculty Advisor or Counselor’ shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites ‘Registration Forms’ from students with in 15 days from the commencement of class work through ‘ON-LINE SUBMISSIONS’, ensuring ‘DATE and TIME Stamping’. The ON-LINE Registration Requests for any ‘CURRENT SEMESTER’ shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the ‘PRECEDING SEMESTER’.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the ‘WRITTEN APPROVAL’ from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries - during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.

4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Subject/ Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new Subject (subject to offering of such a Subject), or for another existing Subject (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

Attendance

The programmes are offered on a unit basis with each subject being considered a unit.

5.1 Attendance in all classes (Lectures/Laboratories etc.) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the days of attendance in sports, games, NCC and NSS activities for appearing for the End Semester examination. A student shall not be permitted to appear for the Semester End Examinations (SEE) if attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee on genuine medical grounds and valid reasons on representation by the candidate with supporting evidence.
5.3 Shortage of Attendance below 65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their end semester examination of that subject and their registration shall stand cancelled.

5.5 A prescribed fees shall be payable towards condonation of shortage of attendance.

5.6 A candidate shall get minimum required attendance at least in three (3) theory subjects in the present semester to get promoted to the next semester. In order to qualify for the award of the M.Tech Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

5.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present Semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

6 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

6.1 For the theory subjects 60 marks shall be awarded for the performance in the Semester End Examination and 40 marks shall be awarded for Continuous Internal Evaluation (CIE). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other, immediately after the completion of Semester instructions. Each mid-term examination shall be conducted for a total duration of 120 minutes with Part A as compulsory question (10 marks) consisting of 5 sub-questions carrying 2 marks each, and Part B to be answered 5 questions carrying 10 marks each. The details of the Question Paper pattern for End Examination (Theory) are given below:

- The Semester End Examination will be conducted for 60 marks. It consists of two parts. i). Part-A for 20 marks, ii). Part-B for 40 marks.

- Part-A is a compulsory question consisting of 5 questions, one from each unit and carries 4 marks each.

- Part-B to be answered 5 questions carrying 8 marks each. There will be two questions from each unit and only one should be answered.

6.2 For practical subjects, 60 marks shall be awarded for performance in the Semester End
Examinations and 40 marks shall be awarded for day-to-day performance as Internal Marks.

6.3 The practical end semester examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed by the Principal from the panel of examiners recommended by Chairman, Board of Studies in respective Branches.

6.4 There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.5 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce is intended to assess the students’ understanding of various subjects he has studied during the M. Tech. course of study. The Head of the Department shall be associated with the conduct of the Comprehensive Viva-Voce through a Committee. The Committee consisting of Head of the Department, one senior faculty member and an external examiner. The external examiner shall be appointed by the Principal from the panel of 3 examiners recommended by Chairman, Board of Studies in respective Branches. There are no internal marks for the Comprehensive Viva-Voce and evaluates for maximum of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to reappear during the supplementary examinations.

6.6 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

6.7 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 6.6) he has to reappear for the Semester End Examination in that subject.

6.8 A candidate shall be given one chance to re-register for the subjects if the internal marks secured by a candidate is less than 50% and failed in that subject for maximum of two subjects and should register within four weeks of commencement of the class work. In such a case, the candidate must re-register for the subjects and secure the required minimum attendance. The candidate’s attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the Semester End Examination in those subjects. In the event of the student taking another chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stands cancelled.

6.9 In case the candidate secures less than the required attendance in any subject, he shall not be permitted to write the Semester End Examination in that subject. He shall re-register for the subject when next offered.
Examinations and Assessment - The Grading System

7.1 Marks will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 6 above, and a corresponding Letter Grade shall be given.

7.2 As a measure of the student’s performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

<table>
<thead>
<tr>
<th>% of Marks Secured (Class Intervals)</th>
<th>Letter Grade (UGC Guidelines)</th>
<th>Grade Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>80% and above</td>
<td>O (Outstanding)</td>
<td>10</td>
</tr>
<tr>
<td>(≥ 80%, ≤ 100%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Below 80% but not less than 70%</td>
<td>A+ (Excellent)</td>
<td>9</td>
</tr>
<tr>
<td>(≥ 70%, &lt; 80%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Below 70% but not less than 60%</td>
<td>A (Very Good)</td>
<td>8</td>
</tr>
<tr>
<td>(≥ 60%, &lt; 70%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Below 60% but not less than 55%</td>
<td>B+ (Good)</td>
<td>7</td>
</tr>
<tr>
<td>(≥ 55%, &lt; 60%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Below 55% but not less than 50%</td>
<td>B (Above Average)</td>
<td>6</td>
</tr>
<tr>
<td>(≥ 50%, &lt; 55%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Below 50%</td>
<td>F (Fail)</td>
<td>0</td>
</tr>
<tr>
<td>(&lt; 50%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Absent</td>
<td>Ab</td>
<td>0</td>
</tr>
</tbody>
</table>

7.3 A student obtaining F Grade in any Subject shall be considered ‘failed’ and is required to reappear as ‘Supplementary Candidate’ in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Subjects will remain the same as those he obtained earlier.

7.4 A student not appeared for examination then ‘Ab’ Grade will be allocated in any Subject shall be considered ‘failed’ and will be required to reappear as ‘Supplementary Candidate’ in the Semester End Examination (SEE), as and when offered.

7.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.
In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of ‘Grade Improvement’ or ‘SGPA/ CGPA Improvement’.

A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding ‘Credit Points’ (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

**Credit Points (CP) = Grade Point (GP) x Credits .... For a Course**

The Student passes the Subject/ Course only when he gets GP \( \geq 6 \) (B Grade or above).

The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (ΣCP) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

\[
SGPA = \frac{\sum_{i=1}^{N} C_i G_i}{\sum_{i=1}^{N} C_i} \text{ For each Semester,}
\]

where ‘i’ is the Subject indicator index (takes into account all Subjects in a Semester), ‘N’ is the no. of Subjects ‘REGISTERED’ for the Semester (as specifically required and listed under the Course Structure of the parent Department), C is the no. of Credits allotted to the ith Subject, and G represents the Grade Points (GP) corresponding to the Letter Grade awarded for that ith Subject.

The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

\[
CGPA = \frac{\sum_{j=1}^{M} C_j G_j}{\sum_{j=1}^{M} C_j} \quad \text{for all S Semesters registered (i.e., upto and inclusive of S Semesters, } S \geq 2 \text{)}.
\]

where ‘M’ is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has ‘REGISTERED’ from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), ‘j’ is the Subject indicator index (takes into account all Subjects from 1 to S Semesters), C is the no. of Credits allotted to the jth Subject, and G represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

For Calculations listed in Item 7.6 – 7.10, performance in failed Subjects/ Courses
(securing F Grade) will also be taken into account, and the Credits of such Subjects/Courses will also be included in the multiplications and summations.

8. **EVALUATION OF PROJECT/DISSERTATION WORK**

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

8.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of 3 months between them.

8.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/School/Institute.

8.8 For Project work **Review I** in II Year I Sem. there is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Work Review I. If he fails to fulfill minimum marks, he has to reappear as per the recommendations of PRC.

8.9 For Project work **Review II** in II Year II Sem. there is an internal marks of 50, the evaluation should be done by the PRC for 25 marks and Supervisor will evaluate for 25 marks. The PRC will examine the overall progress of the Project Work and
decide the Project is eligible for final submission or not. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Work Review II. If he fails to fulfill minimum marks, he has to reappear as per the recommendations of PRC.

8.10 For Project Evaluation (Viva Voce) in II Year II Sem. there is an external marks of 150 and the same evaluated by the External examiner appointed by the Institution. The candidate has to secure minimum of 50% marks in Project Evaluation (Viva-Voce) examination.

8.11 If he fails to fulfill as specified in 8.10, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill, he will not be eligible for the award of the degree.

8.12 The thesis shall be adjudicated by one examiner selected by the Institution. For this, Chairmen, BOS of the respective departments shall submit a panel of 3 examiners, who are eminent in that field with the help of the concerned guide and senior faculty of the department.

8.13 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is un favourable again, the thesis shall be summarily rejected.

8.14 If the report of the examiner is favourable, Project Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis.

8.15 The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva-Voce examination.

9. AWARD OF DEGREE AND CLASS

9.1 A Student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of 88 Credits (with CGPA ≥ 6.0), shall be declared to have ‘QUALIFIED’ for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

9.2 Award of Class

<table>
<thead>
<tr>
<th>Class Awarded</th>
<th>CGPA</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Class with Distinction</td>
<td>≥ 7.75</td>
</tr>
<tr>
<td>First Class</td>
<td>6.75 ≤ CGPA &lt; 7.75</td>
</tr>
<tr>
<td>Second Class</td>
<td>6.00 ≤ CGPA &lt; 6.75</td>
</tr>
</tbody>
</table>

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.
10. **WITHHOLDING OF RESULTS**

If the student has not paid the dues, if any, to the institution or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

11. **TRANSITORY REGULATIONS**

11.1 If any candidate is detained due to shortage of attendance in one or more subjects, they are eligible for re-registration to maximum of two earlier orequivalentsubjects at a time as and when offered.

11.2 The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per R15 Academic Regulations.

12. **GENERAL**

12.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

12.2 **Credit Point**: It is the product of grade point and number of credits for a course.

12.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”.

12.4 The academic regulation should be read as a whole for the purpose of any interpretation.

12.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the Decision of the Academic Council is final.

12.6 The Academic Council may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Academic Council.
## MALPRACTICES RULES

### DISCIPLINARY ACTION FOR IMPROPER CONDUCT IN EXAMINATIONS

<table>
<thead>
<tr>
<th>Nature of Malpractices/Improper conduct</th>
<th>Punishment</th>
</tr>
</thead>
<tbody>
<tr>
<td>If the candidate:</td>
<td></td>
</tr>
<tr>
<td>1. (a) Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, cell phones, pager, palm, computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject only</td>
</tr>
<tr>
<td>(b) Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.</td>
</tr>
<tr>
<td>2. Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.</td>
<td>Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The hall ticket of the candidate is to be cancelled and sent to the controller of examinations, AGI.</td>
</tr>
<tr>
<td>3. Impersonates any other candidate in connection with the examination.</td>
<td>The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination(including practical’s</td>
</tr>
<tr>
<td>No.</td>
<td>Offense</td>
</tr>
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<td>-----</td>
<td>--------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>4</td>
<td>Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.</td>
</tr>
<tr>
<td>5</td>
<td>Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.</td>
</tr>
<tr>
<td>6</td>
<td>Refuses to obey the orders of the Chief Superintendent/Assistant-Superintendent/any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in-charge or any person on duty in or outside the examination hall of any injury to his person or to any office relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations,</td>
</tr>
</tbody>
</table>
or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.

<p>| 7. | Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall. | Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all semester examinations. The continuation of the course by the candidate is subject to the academic regulation in connection with forfeiture of seat. |
| 8. | Posses any lethal weapon or firearm in the examination hall. | Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. |
| 9. | If student of the college, who is not a candidate for the particular examination or any person not connected with college indulges in any malpractice or improper conduct mentioned in clause 6 to 8 | Student of the college’s expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them. |
| 10. | Comes in a drunken condition to the | Expulsion from the examination hall and |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>10.</td>
<td>Examination hall.</td>
<td>Cancellation of performance in that subject and all the other subjects the candidates has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.</td>
</tr>
<tr>
<td>11.</td>
<td>Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.</td>
<td>Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of the semester/year examinations.</td>
</tr>
<tr>
<td>12.</td>
<td>If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the Malpractices committee, AGI for further action to award suitable punishment.</td>
<td></td>
</tr>
</tbody>
</table>
## I YEAR I SEMESTER

### COURSE STRUCTURE

<table>
<thead>
<tr>
<th>Category</th>
<th>Subject</th>
<th>Int. marks</th>
<th>Ext. marks</th>
<th>L</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core course I</td>
<td>Embedded System Design</td>
<td>40</td>
<td>60</td>
<td>4</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>Core course II</td>
<td>Microcontrollers for Embedded System Design</td>
<td>40</td>
<td>60</td>
<td>4</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>Core course III</td>
<td>Embedded Real Time Operating Systems</td>
<td>40</td>
<td>60</td>
<td>4</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>Core Elective I</td>
<td>Advanced Computer Architecture VLSI Technology and Design Embedded Computing</td>
<td>40</td>
<td>60</td>
<td>4</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>Core Elective II</td>
<td>Digital System Design Soft Computing Techniques Advanced Operating Systems</td>
<td>40</td>
<td>60</td>
<td>4</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>Open Elective I</td>
<td>Embedded C Coding Theory and Techniques TCP/IP networks</td>
<td>40</td>
<td>60</td>
<td>4</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>Laboratory I</td>
<td>Embedded C Laboratory</td>
<td>40</td>
<td>60</td>
<td>--</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Seminar I</td>
<td>Seminar</td>
<td>50</td>
<td>--</td>
<td>--</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>24</strong></td>
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## I YEAR II SEMESTER

### COURSE STRUCTURE

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<th>Subject</th>
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### II YEAR I SEMESTER

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### II YEAR II SEMESTER

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UNIT-1:

Introduction to Embedded Systems


UNIT [II]:

Typical Embedded System:

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III:

Embedded Firmware:

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV:

RTOS Based Embedded System Design:

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V:

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:

1. Embedded Systems - Raj Kamal, TMH.
MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT –I:
ARM Architecture:
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:
ARM Programming Model – I:
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:
ARM Programming Model – II:
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:
ARM Programming:
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:
Memory Management:
Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

REFERENCE BOOKS:
EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT – I:
Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II:
Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:
Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:
Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:
REFERENCE BOOKS:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh
ADVANCED COMPUTER ARCHITECTURE
(CORE ELECTIVE -I)

UNIT -I:
Fundamentals of Computer Design:
Fundamentals of Computer design, Changing faces of computing and task of computer designer. Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl’s law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-type and size of operands, Operations in the instruction set.

UNIT –II:
Pipelines:
Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design:

UNIT -III:
Instruction Level Parallelism (ILP) - The Hardware Approach:
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, High performance instruction delivery- Hardware based speculation. ILP Software Approach:
Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV:
Multi Processors and Thread Level Parallelism:
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V:
Inter Connection and Networks:
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

**Intel Architecture:** Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

**TEXT BOOKS:**


**REFERENCE BOOKS:**

VLSI TECHNOLOGY AND DESIGN (CORE ELECTIVE - I)

UNIT –I:
Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:
Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:
Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:
REFERENCE BOOKS:

EMBEDDED COMPUTING
(CORE ELECTIVE – I)

UNIT –I:
Programming on Linux Platform:

UNIT –II:
Introduction to Software Development Tools:
GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

UNIT –III:
Interfacing Modules:
Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT –IV:
Networking Basics:
Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT –V:
IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS:
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals
REFERENCE BOOKS:

2. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
3. UNIX Network Programming by W. Richard Stevens
UNIT -I:

Minimization and Transformation of Sequential Machines:

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.


UNIT -II:

Digital Design:

Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:

SM Charts:

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:

Fault Modeling & Test Pattern Generation:


UNIT -V:

Fault Diagnosis in Sequential Circuits:

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

3. Logic Design Theory – N. N. Biswas, PHI

**REFERENCE BOOKS:**

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SOFT COMPUTING TECHNIQUES(CORE ELECTIVE -II)

UNIT –I:
Introduction:
Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II:
Artificial Neural Networks:
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III:
Fuzzy Logic System:
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV:
Genetic Algorithm:
Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and Ant-colony search techniques for solving optimization problems.

UNIT –V:
Applications:

TEXT BOOKS:

REFERENCE BOOKS:

7. Introduction Neural Networks Using MATLAB 6.0 - S.N. Shivanandam, S. Sumati, S. N. Deepa,1/e, TMH,
UNIT –I:

Introduction to Operating Systems:
Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:

Introduction to UNIX and LINUX:
Basic commands & command arguments, Standard input, output, Input / output redirection, filters and editors, Shells and operations

UNIT –III:

System Calls:
System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication
Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:

Introduction to Distributed Systems:
Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems:
Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:

Synchronization in Distributed Systems:
Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks:
Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.
TEXT BOOKS:
1. The design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.

REFERENCE BOOKS:
UNIT – I

Programming Embedded Systems in C
Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family
Introduction, What’s in a name, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption, Conclusions

UNIT – II:

Reading Switches
Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT – III:

Adding Structure to the Code
Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the ‘Hello Embedded World’ example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT – IV:

Meeting Real-Time Constraints
Introduction, Creating ‘hardware delays’ using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for ‘timeout’ mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT – V:

Case Study: Intruder Alarm System
Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

TEXT BOOKS:


REFERENCE BOOKS:

1. PICmicro MCU C-An introduction to programming, The Microchip PIC in CCS C - Nigel Gardner
UNIT I:
Network Layer Protocols: Internet Protocol (IP), ICMPv4, Mobile IP, IPv6, Addressing IPv6 Protocol,
ICMPV6 Protocol, Transition from IPv4 to IPv6

UNIT II
Transmission Control Protocol: TCP Services, TCP Features, Segments, TCP Connection, State Transition Diagram, Windows in TCP, Flow and Error Control ,TCP Congestion Control, TCP Timers,

UNIT III
User Datagram Protocol: User Datagram, UDP Services, UDP Applications

UNIT IV:
Mobile Network Layer: Entities and Terminology, IP Packet Delivery, Agents, Addressing, Agent Discovery, Registration, Tunneling and Encapsulating, Inefficiency in Mobile IP.

UNIT V:
Congestion Control and Quality of Service: Data Traffic, Congestion, Congestion Control, Quality of Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks
Queue Management: Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection

TEXT BOOKS:
2. Data communication & Networking: B.A. Forouzan, TMH, 5 th
Edition.

REFERENCES:
1. Internetworking with TCP/IP -- Douglas. E.Comer, Volume I PHI -
2. Computer Networks-Larry L. Perterson and Bruce S.Davie -
UNIT – I:
Coding for Reliable Digital Transmission and storage
Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.
Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II:
Cyclic Codes
Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III:
Convolutional Codes
Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT – IV:
Turbo Codes
LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

UNIT - V:
Space-Time Codes
Introduction, Digital modulation schemes, Diversity, Orthogonal space-Time Block codes, Alamouti’s schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing:
General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi-Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS:

REFERENCE BOOKS:
2. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
4. Introduction to Error Control Codes-Salvatore Gravano-oxford
ANURAG GROUP OF INSTITUTIONS (AUTONOMOUS)


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EMBEDDED C LABORATORY

Note:

- Minimum of 10 experiments have to be conducted.
- The following programs have to be tested on 89C51 Development board/equivalent using Embedded C Language on Keil IDE or Equivalent.

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions.
11. Program to Sort RTOS on to 89C51 development board.
12. Program to interface Elevator.

List of Equipment required:

Software:
1. Window 2007
2. Keil IDE
3. Proload V

Hardware
1. 89C51 Development Board
2. PC - IV
UNIT –I:
Co- Design Issues:
Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:
Prototyping and Emulation:
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:
Compilation Techniques and Tools for Embedded Processor Architectures:
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:
Design Specification and Verification:
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:
Languages for System – Level Specification and Design-I:
System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

**TEXT BOOKS:**


**REFERENCE BOOKS:**

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

UNIT –I:

Introduction to Digital Signal Processing:

Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:

Architectures for Programmable DSP Devices:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:

Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:

Analog Devices Family of DSP Devices:


Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:
Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:


REFERENCE BOOKS:

4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
UNIT-I
Embedded Communication Protocols:

UNIT –II:
USB and CAN Bus:

UNIT –III:
Ethernet Basics:

UNIT –IV:
Embedded Ethernet:

UNIT –V:
Wireless Embedded Networking:

TEXT BOOKS:

REFERENCE BOOKS:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
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SENSORS AND ACTUATORS
(CORE ELECTIVE –III)

UNIT -I:

Sensors / Transducers: Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization


UNIT –II:


UNIT -III:

Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors


UNIT -IV:


UNIT -V:

**Actuators:** Pneumatic and Hydraulic Actuation Systems - Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators

Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection


**TEXT BOOKS:**


**REFERENCE BOOKS:**

ANURAG GROUP OF INSTITUTIONS
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M. Tech – I Year – II Sem.

WIRELESS COMMUNICATIONS AND NETWORKS
(CORE ELECTIVE –III)

UNIT -I:


UNIT–II:


UNIT –III:

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke’s model for flat fading, spectral shape due to Doppler spread in Clarke’s model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT-IV

Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT -V:

**Wireless Networks**: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11, IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL.

**TEXT BOOKS:**


**REFERENCE BOOKS:**

M. Tech – I Year – II Sem.  L  P  C
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NETWORK SECURITY AND CRYPTOGRAPHY
(CORE ELECTIVE – III)

UNIT –I:


UNIT –II:

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.


Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.


UNIT –III:

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat’s and Euler’s theorems, Testing for primality, Euclid’s Algorithm, the Chinese remainder theorem, Discrete logarithms.


UNIT –IV:


UNIT –V:

**IP Security:** Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

**Web Security:** Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

**Intruders, Viruses and Worms:** Intruders, Viruses and Related threats.

**Fire Walls:** Fire wall Design Principles, Trusted systems.

**TEXT BOOKS:**


**REFERENCE BOOKS:**

1. Fundamentals of Network Security by Eric Maiwald (Dreamtech press)
4. Introduction to Cryptography, Buchmann, Springer.
MULTI MEDIA AND SIGNAL CODING
(CORE ELECTIVE -IV)

UNIT -I:


UNIT -II:

**Video Concepts:** Types of Video Signals, Analog Video, Digital Video.

**Audio Concepts:** Digitization of Sound, Quantization and Transmission of Audio.

UNIT -III:

**Compression Algorithms:**

**Lossless Compression Algorithms:** Run Length Coding, Variable Length Coding, Arithmetic Coding, Lossless JPEG, Image Compression.

**Lossy Image Compression Algorithms:** Transform Coding: KLT And DCT Coding, Wavelet Based Coding.

**Image Compression Standards:** JPEG and JPEG2000.

UNIT -IV:

**Video Compression Techniques:** Introduction to Video Compression, Video Compression Based on Motion Compensation, Search for Motion Vectors, H.261- Intra-Frame and Inter-Frame Coding, Quantization, Encoder and Decoder, Overview of MPEG1 and MPEG2.

UNIT -V:

TEXT BOOKS:


REFERENCE BOOKS:

5. Video Processing and Communications – Yaowang, Jorn Ostermann, Ya-QinZhang, Pearson, 2002
ANURAG GROUP OF INSTITUTIONS
(AUTONOMOUS)

M. Tech – I Year – II Sem.

SYSTEM ON CHIP ARCHITECTURE
(CORE ELECTIVE -IV)

UNIT –I:
Introduction to the System Approach:

UNIT –II:
Processors:

UNIT –III:
Memory Design for SOC:

UNIT -IV:
Interconnect Customization and Configuration:

UNIT –V:
Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.
TEXT BOOKS:


REFERENCE BOOKS:

2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
UNIT –I:  
Wireless System & Random Access Protocols: 

UNIT –II: 
Wireless LANs: 
Introduction, importance of Wireless LANs, WLAN Topologies, Transmission Techniques: Wired Networks, Wireless Networks, comparison of wired and Wireless LANs; WLAN Technologies: Infrared technology, UHF narrowband technology, Spread Spectrum technology

UNIT –III:  
The IEEE 802.11 Standard for Wireless LANs:  
Network Architecture, Physical layer, The Medium Access Control Layer; MAC Layer issues: Hidden Terminal Problem, Reliability, Collision avoidance, Congestion avoidance, Congestion control, Security, The IEEE 802.1 1e MAC protocol

UNIT –IV:  
Wireless PANs:  
Introduction, importance of Wireless PANs, The Bluetooth technology: history and applications, technical overview, the Bluetooth specifications, piconet synchronization and Bluetooth clocks, Master-Slave Switch; Bluetooth security; Enhancements to Bluetooth: Bluetooth interference issues, Intra and Inter Piconet scheduling, Bridge selection, Traffic Engineering, QoS and Dynamics Slot Assignment, Scatternet formation.

UNIT –V:  
The IEEE 802.15 working Group for WPANs:  
The IEEE 802.15.3, The IEEE 802.15.4, ZigBee Technology, ZigBee components and network topologies, The IEEE 802.15.4 LR-WPAN Device architecture: Physical Layer, Data Link Layer, The Network Layer, Applications; IEEE 802.15.3a Ultra wideband.
TEXT BOOKS:


REFERENCE BOOKS:

UNIT-I:
Introduction to Programmable Logic Devices:

UNIT-II:
Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:
SRAM Programmable FPGAs:

UNIT -IV:
Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:
Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:
1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer

**REFERENCE BOOKS:**

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
AD-HOC WIRELESS AND SENSOR NETWORKS
(Open Elective -II)

UNIT - I:
Wireless Local Area Networks
Introduction, wireless LAN Topologies, Wireless LAN Requirements. Physical Layer-Infrared Physical Layer, Microwave based Physical Layer Alternatives, Medium Access Control Layer- HIPERLAN 1 Sublayer, IEEE 802.11 MAC Sublayer and Latest Developments-802.11a, 802.11b, 802.11g

UNIT - II:
MAC Protocols

UNIT - III:
Routing Protocols

UNIT – IV:
Transport Layer Protocols
UNIT – V:

Wireless Sensor Networks


TEXT BOOKS:


REFERENCE BOOKS:


UNIT -I:

Introduction to Semiconductor Physics:

Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation. Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II:

Integrated Diodes:

Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon modeldynamic model, Parasitic effects – SPICE model – Parameter extraction

UNIT -III:

Integrated MOS Transistor:

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV:

VLSI Fabrication Techniques:


UNIT -V:

Modeling of Hetero Junction Devices:

Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe
TEXT BOOKS:


REFERENCE BOOKS:

EMBEDDED SYSTEMS LABORATORY

Note:

The following programs are to be implemented on ARM based Processors/Equivalent. Minimum of 10 programs from Part –I and 6 programs from Part -II are to be conducted.

PART- I:

The following Programs are to be implemented on ARM Processor

1. Simple Assembly Program for
   - Addition | Subtraction | Multiplication | Division
   - Operating Modes, System Calls and Interrupts
   - Loops, Branches
2. Write an Assembly programs to configure and control General Purpose Input/Output (GPIO) port pins.
3. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
4. Program for reading and writing of a file
5. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
6. Program to demonstrates a simple interrupt handler and setting up a timer
7. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
8. Program to Interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment
10. Program to Displaying a message in a 2 line x 16 Characters LCD display and verify the result in debug terminal.
11. Program to demonstrate I2C Interface on IDE environment
12. Program to demonstrate I2C Interface – Serial EEPROM
13. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program.
14. Generation of PWM Signal
15. Program to demonstrate SD-MMC Card Interface.

PART- II:

Write the following programs to understand the use of RTOS with ARM Processor on IDE Environment using ARM Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
   a). Write an application to Test message queues and memory blocks.
a. b). Write an application to Test byte queues

5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.

**Interfacing Programs:**

6. Write an application that creates a two task to blinking two different LEDs at different timings.
7. Write an application that creates a two task displaying two different messages in LCD display in two lines.
8. Sending messages to mailbox by one task and reading the message from mailbox by another task.
9. Sending message to PC through serial port by three different tasks on priority Basis.
10. Basic Audio Processing on IDE environment.

**List of Equipment required:**

**Software:**
1. Window 2007
2. Keil IDE
3. Flash Magic

**Hardware**
1. ARM 7 Development Board
2. PC -IV