PROGRAM STRUCTURE

AND

DETAILED SYLLABUS

R20 REGULATIONS

M.Tech (VLSI SYSTEM DESIGN)

FOR
MASTER OF TECHNOLOGY TWO YEAR POST GRADUATE COURSE
(Applicable for the batches admitted from 2020-2021)

ANURAG UNIVERSITY

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Academic Regulations for M. Tech. (Regular) with effect from the Academic Year 2020-21

1. Eligibility for Admissions

1.1 Admission to the M.Tech. program shall be made subject to eligibility, qualification and specialization as prescribed by the Anurag University (AU) from time to time.

1.2 Admissions shall be made on the basis of merit / rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as prescribed by the Telangana State Private Universities Act (Establishment and Regulations) No.11 of2018.

2. Courses of Study

The following specializations are offered for the M.Tech program of study:

1. Computer Science and Engineering
2. Electrical Power Systems
3. Embedded Systems
4. Machine Design
5. Power Electronics and Electrical Drives
6. Structural Engineering
7. VLSI System Design

3. Course Registration

3.1 Every student is required to be present and register online at the commencement of each semester on the day fixed for and notified in the academic calendar. The students will choose the courses for registration in consultation with the Faculty Advisor. The students may also consult the Head of the Department / Dean of the School.

3.2 The registration will be organized departmentally under the supervision of the Head of the Department in coordination with Faculty Advisor.

3.3 A student, who does not register on the day announced, may be permitted to register, in consideration of any compelling reason, within the first week. Similarly, a student may be permitted to change the registration for a course within the first week only in consultation with respective faculty advisor. No late registration/change of registration shall be permitted after the first week

from the scheduled date.

3.4 Only those students will be permitted to register who have: (a) cleared all University and Hostel dues of the previous semesters (b) paid all required fees for the current semester, and (c) not been debarred from registering for a specified period on disciplinary action or any other ground.

3.5 A candidate shall be given one chance to re-register and attend the classes for a maximum of two courses, if the CIE marks secured by a candidate are less than 50% and failed in those subjects but fulfilled the attendance requirement. A candidate must re-register for failed courses within four weeks of commencement of the class work and secure the required minimum attendance to appear for SEE. In the event of the student taking this chance, his CIE marks and SEE marks obtained in the previous attempt stand cancelled.

3.6 Dropping of courses: Within four weeks after the commencement of the semester, the student may, in consultation with the faculty advisor, drop one or more courses. The dropped courses shall be registered in the subsequent semesters as and when it is offered.

4. Attendance

4.1 Attendance in all classes (lectures/tutorials, laboratories etc.) is compulsory. A student will not be permitted to appear in the semester end examination on grounds of unsatisfactory attendance. Minimum required attendance in each theory / laboratory course is 75% (including the days of attendance in sports, games, and NCC and NSS activities) for appearing in the semester end examination. Students are advised to monitor the status of their attendance in the online system from time to time. Absence without obtaining sanction of leave will be considered as an act of indiscipline.

4.2 Condonation of shortage of attendance in each course up to 10% (65% and above and below 75%) in each semester shall be granted on genuine medical grounds and valid reasons on representation by the candidate with supporting documentary evidence.

4.3 Shortage of attendance below 65% in each course shall not be condoned.

4.4 Students whose shortage of attendance is not condoned in any course are not eligible to appear for their semester end examination of that course and their registration shall stand cancelled.

4.5 However, in respect of women candidates who seek condonation of attendance due to pregnancy, the Vice-Chancellor may condone the deficiency in

attendance to the extent of 15% (as against 10% condonation for others) on medical grounds subject to submission of medical certificate to this effect. Such condonation shall be availed only twice during the program of study.

4.6 A prescribed fee shall be payable towards condonation of shortage of attendance.

4.7 A candidate shall get minimum required attendance atleast in three (3) theory courses in the present semester to get promoted to the next semester.

4.8 PromotionRules:

4.8.1 A student shall be promoted from I Year to II Year only if he/she fulfills the academic requirements of securing 50% of average credits up to I Year II Semester, from all the examinations, whether or not the candidate takes the examinations.

4.8.2 A student shall register and put up required attendance in all 88 credits and earn all 88 credits for the award ofdegree.

4.8.3 Students, who fail to earn 88 credits as indicated in the course structure within four academic years from the year of their admission, shall forfeit their admission.

4.9 When a student is detained due to shortage of attendance in any semester, no grade allotments or SGPA/CGPA calculations will be done for that entire semester in which he/she got detained.

4.10 When a student is detained due to lack of credits in any year, he / she may be readmitted after fulfillment of the academic requirements, with the academic regulations of the batch into which he / she gets readmitted.

4.11 For readmitted candidates, if there are any professional electives / open electives, the same may also be re-registered if offered. However, if those electives are not offered in later semesters, then alternate electives may be chosen from the set of elective courses offered under that category.

5. Assessment of Academic Performance

5.1 The performance of a student in a semester shall be evaluated course-wise for a maximum of 100 marks in each theory and practical course. In addition, Seminars, Comprehensive Viva-Voce, Technical Paper writing, Project Work Reviews and Project Work shall be evaluated for 100 marks each. The distribution of marks for Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE) along with the minimum pass percentage shall be as follows:

Course	Continuous Internal Evaluation (CIE)	Semester End Examination (SEE)	Minimum Requirements to	academic Pass a Course
			*Minimum Pass Percentage (SEE)	*Minimum Pass Percentage (CIE+SEE)
Theory	40	60	40	50
Laboratory / Practicals	50	50	40	50
Seminars	100	0	-	50
Comprehensive Viva-Voce	-	100	50	**50**
Technical Paper Writing	100	-	-	50
Project Reviews	100	-	-	50

*Provided a relaxation of 10% of maximum marks shall be given to physically challenged students.

5.2 Each theory course in a semester is evaluated for 100 marks, with the following weightages:

5.2.1 Continuous Internal Evaluation(CIE)

The CIE for Theory Courses has the following three components, comprising of 40 marks:

a. Midterm Examinations for 20marks

b. Quizzes for 10marks

c. Assignment / Seminars / Projects / Group Activities for10 marks

a. Mid-term Examinations

There shall be two midterm examinations of 20 marks each. The average of the two examinations shall be taken as the marks secured by each candidate. Each midterm examination shall be conducted for the duration of 90 minutes and the question paper consists of Part-A (Short Answers for 5 marks) consists of 5 questions carrying 1 mark each, and Part-B (Long Answers for 15 marks) containing 5 questions of which student has to answer 3 questions; each question carrying 5 marks.

The First midterm examination shall be conducted for 2.5 units of syllabus at the end of 8 weeks of instruction and Second midterm examination shall be conducted for remaining 2.5 units at the end of 16 weeks of instruction.

In case any student has missed one of the two examinations, or wants to improve in one of the examinations, an optional third midterm examination

will be conducted. This optional third midterm examination will be conducted during the preparation cum external practical examinations period subject to the following conditions:

1. Interested students have to register for the third mid examination by paying the prescribed registration fee.
2. Third midterm examination covers entire semester syllabus carrying 20marks

b. Quizzes:

There shall be a total of five quizzes of 10 marks each. The quiz is to be conducted at the end of each of the five units of instruction. The average of the five quizzes shall be taken as the final marks secured by each candidate.

5.2.2 Assignment / Seminars / Projects / Group Activities:

The faculty will evaluate the students for 10 marks by conducting any of the following in two phases covering atleast two units in each phase: Assignments / Seminars / Projects / Group Activities. This should be completed before the conduct of second mid-term examination.

This should be completed before the conduct of the second midterm examination.

5.2.3 Semester End Examination

c. The semester end examination will be conducted for 60 marks. The question paper will consist of two parts viz.,i) Part-A for 20marks, ii) Part –B for 40 marks.

d. Part-A is compulsory, which consists of ten questions (numbered from 1 to 10), two questions from each unit carrying 2 marks each.

e. Part-B consists of five questions (numbered from 11 to 15) shall be set by covering one question (may contain sub-questions) from each unit of the syllabus carrying 8 marks each. For each question there will be an“either”“or”choice (that means there will be two questions from each unit and the student shall have to answer any one of them).

5.3 Each laboratory course in a semester is evaluated for 100 marks, with the following weightages:

a. Throughout the semester the student will be evaluated for 50 marks under CIE as follows**:**

i. Preparation for Lab – 10 marks.
ii. Observation – 10 marks.
iii. Completion of Experiment – 5 marks.
iv. Record –5 marks.
v. Skill Test – 20 Marks

Before the end of instruction a Skill Test will be conducted for 20 marks. The practical SEE shall be conducted for 50 marks with an examiner along with the lab faculty. The examiner shall be appointed by the Dean (Examinations) of the University.

5.4 There shall be two seminar presentations during I Year I Semester and I Year II Semester. For each Seminar there will be only internal evaluation of 100 marks. Students shall present a seminar before the faculty members assigned for the purpose.

5.5 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce is intended to assess the students' understanding of various courses he has studied during the program. Comprehensive viva-voce will be taken by the faculty members assigned for the purpose.

5.6 There shall be a Technical Paper Writing that covers concepts of abstract, introduction, material and methods, conclusion, references, acknowledgement etc. The report shall be presented as a printed document for evaluation. Evaluation shall done by the faculty member assigned for the purpose

5.7 There shall be a project work review I and II in 2nd Year first and second semester respectively. For the Project work Reviews there is an internal marks of 100, the evaluation should be done by the Project Review Committee (PRC) for 50 marks and Supervisor will evaluate for 50 marks.

5.8 A candidate shall be given one chance to re-register for the courses if the internal marks secured by a candidate is less than 50% and failed in that course for maximum of two times. In the event of the student taking another chance, his / her CIE and SEE marks obtained in the previous attempt stands cancelled.

5.9 If there is a complaint in awarding the CIE marks, the University shall nominate a committee to look into the matter.

5.10 Candidates shall be permitted to apply for recounting/revaluation of SEE theory-scripts within the stipulated period with payment of prescribed fee.

5.11 Recounting: The totaling of the marks awarded shall be verified in the answer script and corrected if there is any mistake.

5.12 Revaluation

a) The answer scripts of the candidate who applied for revaluation are evaluated by two subject experts independently other than the original evaluator.

b) If the difference of marks between these two valuations is 15% or more, it will be sent for third valuation to another subject expert.

c) Nearest of two valuations out of three will be considered and the average of these two will be taken as the final marks obtained.

d) If the difference of the final marks and original marks after revaluation is 15% or more of maximum marks, then the revaluation marks are considered for declaring the result.

e) If the revaluation marks are less than the original marks, the original marks are retained and there is no change in the result.

5.13 Challenge Valuation:

The candidates who have applied for revaluation and are not satisfied with the result are only eligible to apply for challenge valuation by paying the prescribed fee in the form of DD payable to the Registrar, AU.

a) On receipt of the DD, a photocopy of the answer booklet shall be given to the student.

b) The paper will be evaluated in the presence of the student by a senior faculty member appointed by the University.

c) If there is any change in the marks >= 15% of the maximum marks, the new marks will be awarded to the student. Otherwise, there will be no change in original secured marks.

d) If the change in marks (equal or above 15% of the maximum marks) occurs, the amount paid towards challenge valuation will be refunded.

Otherwise, the student will forfeit the total amount which he/she has paid.

6. The Grading System

6.1 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and Corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	Letter Grade (as per UGC Guidelines)	Grade Points
90% and above (≥ 90%, ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (≥ 80%, < 90%)	**A**$^{+}$(Excellent)	9
Below 80% but not less than 70% (≥ 70%, < 80%)	**A** (Very Good)	8
Below 70% but not less than 60% (≥ 60%, < 70%)	**B**$^{+}$(Good)	7
Below 60% but not less than 50% (≥ 50%, < 60%)	**B** (Above Average)	6
Below 50% (< 50%)	F (Fail)	0
Absent	Ab	0

6.2 In general, a student shall not be permitted to repeat any course(s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA improvement'.

6.3 The 'Credit Points' (CP) for a course, is computed by multiplying the Grade Point with Credits for that particular course.

Credit Points (CP) = Grade Point (GP) x Credits

6.4 The Student passes the course only when he/she gets GP □6 (B Grade or above).

6.5 The Semester Grade Point Average (SGPA) is calculated as follows

$$SGPA = \frac{\{\sum_{i=1}^{N} C_i G_i\}}{\{\sum_{i=1}^{N} C_i\}}$$

where 'i' is the course indicator index (takes into account all courses in a semester), 'N' is the no. of courses registered for the Semester (as specifically required and listed under the Course Structure of the parent Department), C is the no. of Credits allotted to the i^{th} course, and G represents the Grade Points (GP) corresponding to the Letter Grade awarded for that course.

6.6 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all semesters considered for registration. The CGPA is calculated as follows:

$$CGPA = \frac{\{\sum_{j=1}^{M} C_j G_j\}}{\{\sum_{j=1}^{M} C_j\}}$$

Where 'M' is the total no. of courses (as specifically required and listed under the course Structure of the parent Department) the Student has registered from the 1st Semester onwards up to and inclusive of the Semester S (obviously M > N), 'j' is the course indicator index (takes into account all courses from 1 to S Semesters), C is the no. of credits allotted to the j^{th} course, and G represents the Grade Points (GP) corresponding to the Letter Grade awarded for that j^{th} course. After registration and completion of I Year I Semester however, the SGPA of that semester itself may be taken as the CGPA, as there are no cumulative effects.

6.7 For CGPA and SGPA calculations performance in failed courses (securing F Grade) will also be taken into account, and the Credits of such courses will also be included in the multiplications and summations.

7. Passing Standards

7.1 A student shall be declared successful or 'passed' in a Semester, only when he/she gets a SGPA ≥ 6.00 (at the end of that particular Semester); and a student shall be declared successful or 'passed' in the entire UGP, only when he/she gets a CGPA ≥ 6.00; subject to the condition that he/she secures a GP ≥ 6 (B Grade or above) in every registered course in each Semester.

7.2 After the completion of each semester, a grade card or grade sheet (or transcript) shall be issued to all the registered students of that semester, indicating the letter grades and credits earned. It will show the details of the courses registered (course code, title, No. of credits, grade earned etc.), credits earned, SGPA and CGPA.

8. Evaluation of Project/Dissertation Work

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

8.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairman, Project Supervisor and two senior faculty members.

8.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical.

8.3 After satisfying 8.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

8.4 If a candidate wishes to change his supervisor or topic of the project, he/she can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

8.5 A candidate shall submit his project status report in two stages at least with a gap of 3 months between them.

8.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

8.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the University.

8.8 After approval from the PRC, a soft copy of the thesis should be submitted for PLAGIARISM check and the plagiarism report should be submitted to the examination branch and be included in the final thesis. The thesis will be accepted for submission, if the similarity index is less than 30%. If the similarity index has more than the required percentage, the student is advised to modify accordingly and re-submit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to TWO. The candidate has to register for the project work and work for two semesters. After two attempts, the admission is liable to be cancelled.

8.9 For Project Evaluation (Viva Voce) in II Year II Sem. there is an external mark of 100 and the same evaluated by the External examiner appointed by the Institution. The candidate has to secure minimum of 50% marks in Project Evaluation (Viva-Voce) examination.

8.10 If he/she fails to fulfill the condition as specified in 8.9, he/she shall reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill the above said condition, he/she will not be eligible for the award of the degree.

8.11 The thesis shall be adjudicated by one examiner appointed by the Dean-Examinations from the list of panel of examiners approved by the Vice-Chancellor. For this, Chairman, Board of Studies of the respective departments shall submit a panel of 3 examiners, who are eminent in that field with the help of the concerned guide and senior faculty of the department.

8.12 If the report of the examiner is unfavorable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

8.13 If the report of the examiner is favorable, Project Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis.

8.14 The Head of the Department shall coordinate and make arrangements for the conduct of Project Viva-Voce examination.

9 Award of Degree and Class

9.1 A Student who registers for all the specified courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Program (PGP), and secures the required number of Credits 88 (with CGPA $\geq$ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech Degree in the chosen Branch of Engineering and Technology with specialization as he/she admitted.

9.2 Award of Class

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M.Tech Degree, he/she shall be placed in one of the following three classes based on the CGPA:

CGPA	Class	Condition
≥8.00	First Class with Distinction	• Should have passed all the courses in 'first appearance' in a semester examinations and should complete the program in 2 years of time. • Should not have been detained or prevented from writing the end semester examinations in any semester due to shortage of attendance or any other reason.
≥6.75 - <8.00	First Class	• The Students who secure CGPA≥8.00 , but not fulfilling above conditions for "First Class with Distinction" shall be awarded "First Class"
≥ 6.00 -< 6.75	Second class	

9.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

10 Withholding of Results

If the student has not paid the dues, if any, to the institution or if any case of indiscipline is pending against him/her, the result of the student will be withheld and he/she will not be allowed into the next semester. His/her degree will be withheld in such cases.

11 Transitory Regulations

11.1 Discontinued, detained or failed candidates are eligible for readmission / re-registration as and when offered next as per the University admission procedure.

11.2 The candidate who fails in any course has to complete the same course / equivalent course in the maximum stipulated time as per the Regulations in vogue.

12 Convocation

12.1 The University shall conduct convocation to confer the degree(s).

12.2 The University shall institute Prizes and Awards to meritorious students during convocation.

13 Amendments

The regulations hereunder are subject to amendments as may be made by Academic Council from time to time. Any or all such amendments will be effective from such date and to such batches of candidates (including those already undergoing the program).

ANNEXURE – I: Disciplinary Action against Students – Provisions

A. Student's behavior and discipline will be assessed and will receive the same attention as the academic work. Discipline includes the observance of good conduct and orderly behavior by the students of the University;

B. All students pursuing a Program at the University shall observe code of conduct and maintain discipline and must consider it as a duty to behave decently at all places;

C. Every student shall always carry the Identity card issued by the university. Every student shall have to produce or surrender the identity card, as and when required by the proctorial staff, teaching and library staff and the officials of the university. The loss of the identity card, whenever it occurs, shall immediately be reported in writing to the Registrar.

D. Any violation of the code of conduct or breach of any rules and regulations of the university is construed as an act of indiscipline and shall make him/her liable for disciplinary action;

E. The following acts are treated as gross indiscipline;

   a) Disobeying the teacher/officials or misbehaving in the class;
   b) Quarrelling or fighting in the University campus, hostels amongst themselves, indulging in any activity which amounts to ragging or Harassment of other students;
   c) Quarrelling or fighting with a University employee(s) or any other public utility functionaries in the campus;
   d) Indecent behavior in the University campus or outside causing inconvenience to others;
   e) Visiting socially unacceptable websites, smoking or consuming liquor or banned substances like drugs etc. ;
   f) Damage to the University property;
   g) Indulging in acts of theft, forgery, stealing and misappropriating;
   h) Any other activity that defames the University;
      i. Use of mobile in the class/academic area.
      ii. irregularity in attending classes, persistent idleness, negligence or indifference towards the work assigned;
      iii. Any other conduct which is considered to be unbecoming of a student.

F. Rules for Students Conduct & Behavior in Campus and Outside;

G. The rules and regulations, academic calendar shall be provided to all the students

H. In general, Dean, Student Affairs will deal with the welfare and discipline of all students in the campus including Hostel and also outside the campus and will ensure maintenance of good conduct. He/ She will be assisted by other members of faculty/ staff/ wardens as nominated;

I. Conduct and Behavior:

a) Students should attend all their classes and strictly observe class timings. They should likewise carry out other out-door and extracurricular duties assigned to them. Their attendance and leave is governed by the regulations pertaining to them;

b) Students must give their undivided attention to their academic work and must be respectful to their teachers and supervisors;

c) Students must conduct themselves with due decorum in the classes, laboratories, Library etc. and move in an orderly and disciplined manner in the campus;

d) Students should not indulge in abusive behavior/ violence of any kind with fellow students, teaching faculty and employees of the University within or outside the University. Violence by any student or group of students will lead to severe disciplinary action;

e) No meeting of the students other than those organized under the aegis of the various recognized students' activities shall be called without the prior permission in writing from the Dean, Student Affairs;

f) Neither meetings/functions within the University campus shall be organized nor any outsider address the students without the prior permission in writing from the Registrar;

g) No students shall use unfair means at any of the examinations and tests or attempt or threaten the staff to get undue advantage;

h) Students must pay all fees and other dues on specified dates. If they do not do so, they render themselves liable to penalties as in force from time to time;

i) Students must take good care of all University property. Any damage to University property shall be viewed as indiscipline. Such student(s), in addition to facing the disciplinary action, shall have to replace the damaged property and make good the losses caused due to their action. Students must use the furniture and fittings with due care and must not deface buildings, roads, furniture and fittings etc. in any manner;

j) Students must handle the laboratory equipment, instruments and machinery with great care. Any damage or breakage of such equipment etc., due to improper use are negligent handling will have to be made good by the students concerned;

k) Ragging in any form is unlawful and strictly prohibited. If a student found ragging shall be punished as per the Anti-Ragging Act;

l) The University shall have a zero-tolerance policy towards Ragging and shall lay down strict guidelines on the same as per policies of the UGC in vogue and in compliance to directions of Hon’ble Supreme Court;

m) Mobile cellular phone may be carried by the students. However, they shall be kept in silent mode during the classes. Violation will lead to confiscation of the mobile phone;

n) All the students are required to observe the decorum in the dress code as prescribed by the University. Students not adhering to the prescribed dress code may be denied entry to the University campus;

o) Smoking, consumption/possession of liquor, intoxicants, drugs, cigarettes, hookah etc., inside or outside the Campus is strictly prohibited. Any violation will invoke severe penalty including rustication from the Hostel/ University.

J. Policy to prevent Sexual Harassment:

a) The University shall be committed to treating every employee and student with dignity and respect. It shall seek to create a work environment that is free from sexual harassment of any kind, whether verbal, physical or visual;

b) A policy shall be prescribed by the University to provide guidelines for prompt redressal of complaints related to sexual harassment which should be in full compliance with "The Sexual Harassment of Women at Workplace (Prevention, Prohibition & Redressal)" Act, 2013;

c) All references / complaints and redressal mechanism pertaining to any matter will be handled within the ambit of the said Act and the Rules framed thereunder. The policy so prescribed shall be communicated to all employees and students.

K. Grievance and Redressal Mechanisms:

The University shall constitute various Grievance and Redressal committees and its guidelines as specified by the statutory authorities of the University.

ANNEXURE – II: Malpractices Rules

S.No	Nature of Malpractice Improper conduct during examinations	Punishment
	***If the candidate*:**	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he/she is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he/she will be handed over to the police and a case is registered against him/her.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate disappearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The hall ticket of the candidate is to be cancelled.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all Semester end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he/she will be handed over to the police and a case is registered against him/her.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination. Takes away answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all SEEs. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks	Cancellation of the performance in that subject.
6	Refuses to obey the orders of the Chief Superintendent / Assistant Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty inside or outside the examination hall or causing any injury to himself / herself or to any others or threatens whether by words, either spoken or written or by signs or by visible representation, assaults the officer in-charge, or any person on duty in or outside the examination hall or any others, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	They shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case will be registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears the script or any part-thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work & shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all Semester examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits these at.
9.	Who is not a candidate for the particular examination or any person not connected with the University indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the University will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Found copying,on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the malpractice committee for further action on suitable punishment as per rules.	

ANNEXURE –III: Definitions

In these Regulations, unless the context otherwise requires:

a. Academic Year: Two consecutive (one odd + one even) semesters constitute one academic year

b. Choice Based Credit System (CBCS): The CBCS provides choice for students to select from the prescribed courses (core, elective or minor or soft skill courses)

c. Course: Usually referred to, as a 'course' is a component of a program. All courses neednot carry the same weightage. The courses should define learning objectives and learning outcomes. A course may be designed to comprise lectures/tutorials/laboratory work/field work/outreach activities/ project work/vocational training/viva/seminars/term papers/assignments/ presentations/self- study etc., or a combination of some of these

d. Credit Based Semester System (CBSS): Under the CBSS, the requirement for awarding a degree or diploma or certificate is prescribed in terms of number of credits to be completed by the students

e. Credit: A unit by which the course work is measured. It determines the numberof hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week

f. Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale

g. Credit Point: It is the product of grade point and number of credits for a course

h. Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters i.e., O, A+, A, B+, B, C and F

i. Semester Grade Point Average (SGPA): It is a measure of academic performance in a semester. It is the ratio of total credit points secured by a student in various courses registered in a semester and the total course credits taken during that semester. It shall be expressed up to two decimal places

j. Cumulative Grade Point Average (CGPA): It is a measure of overall cumulative performance of a student. The CGPA is the ratio of total credit points secured by a student in all semesters and the sum of the total credits. It shall be expressed up to two decimal places

k. Program: An academic program of the University

l. Semester: Each semester shall consist of 16 weeks of instruction.

m. Transcript or Grade Card or Certificate: Based on the grades earned, a grade certificate shall be issued to all the registered students after every semester. The grade certificate will display the course details (code, title, number of credits, grade secured) along with SGPA of that semester and CGPA earned till that semester

n. Types of courses: The courses in a program may be of three kinds: Core, Elective and Foundation

o. Core course: This is the course which is to be compulsorily studied by a student as a core requirement of a program in a branch of study

p. Elective course: This is the course to be chosen from a pool of courses. Elective course may be (a) Supportive to the branch of study (b) Providing an expanded scope (c) Enabling an exposure to some other branch/domain (d) Nurturing student's proficiency/skill

q. Foundation course:This course may be of two kinds, compulsory foundation and elective foundation

r. Compulsory Foundation courses: These are the courses based upon the content that leads to knowledge enhancement. They are mandatory for all disciplines

s. Elective Foundation courses: These are value-based and are aimed at man-making education

t. The academic regulations should be read as a whole for the purpose of any interpretation.

u. In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chancellor is final.

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COURSE STRUCTURE

I SEMESTER

CODE	Category	Course Title	L	T	P	C
A31051	**PC-I**	Advanced Digital System Design	**4**	**0**	**0**	**4**
A31052	**PC-II**	VLSI design verification and testing	**4**	**0**	**0**	**4**
A31053	**PC-III**	CMOS Analog IC Design	**4**	**0**	**0**	**4**
A31054 A31055 A31056	**PE-I**	CMOS Digital IC Design Hardware Software Co-Design CPLD and FPGA Architectures and Applications	**3**	**0**	**0**	**3**
A31057 A31058 A31059	**PE-II**	Algorithms for VLSI Design Automation Embedded System Design Advanced Computer Architecture	**3**	**0**	**0**	**3**
A31060 A31061	**OE-1**	*Open Elective – I	**3**	**0**	**0**	**3**
A31213	**Lab-I**	Digital IC Design Lab	**0**	**0**	**3**	**2**
A31214	**Seminar-I**	Seminar – I	**0**	**0**	**3**	**2**
Total			**21**	**0**	**6**	**25**

II SEMESTER

CODE	Category	Course Title	L	T	P	C
A32047	**PC-IV**	Low Power VLSI Design	**4**	**0**	**0**	**4**
A32048	**PC-V**	Design for Testability	**4**	**0**	**0**	**4**
A32049	**PC-VI**	Full custom IC Design	**4**	**0**	**0**	**4**
A32050 A32051 A32052	**PE-III**	VLSI and DSP Architectures CMOS Mixed Signal Circuit Design Device modeling	**3**	**0**	**0**	**3**
A32053 A32054 A32055	**PE-IV**	RF IC Design System On Chip Architecture Scripting Languages	**3**	**0**	**0**	**3**
A32056 A32057	**OE-II**	*Open Elective – II	**3**	**0**	**0**	**3**
A32214	**Lab-II**	ASIC CAD Lab	**0**	**0**	**3**	**2**
A32215	**Seminar-II**	Seminar – II	**0**	**0**	**3**	**2**
Total			**21**	**0**	**6**	**25**

III SEMESTER

CODE	Course Title	L	T	P	C
A33213	Technical Paper Writing	**0**	**3**	**0**	**2**
A33214	Comprehensive Viva-Voce	**0**	**0**	**0**	**4**
A33215	Project work Review II	**0**	**0**	**22**	**8**
Total		**0**	**3**	**22**	**14**

IV SEMESTER

CODE	Course Title	L	T	P	C
A34209	Project work Review III	**0**	**0**	**24**	**8**
A34210	Project Evaluation (Viva-Voce)	**0**	**0**	**0**	**16**
Total		**0**	**0**	**24**	**24**

NOTE: *Open Elective subjects must be chosen from the list of open electives offered by other departments.

Open elective offered for other department

1. Principles of Electronic Communications
2. Embedded system design
3. Principles of computer communications and networks
4. Industrial instrumentation

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M. Tech – I Year – I Sem	**L**	**P**	**C**
	4	**0**	**4**

ADVANCED DIGITAL SYSTEM DESIGN (PC-1)

UNIT - I

Processor Arithmetic: Two's Complement Number System - Arithmetic Operations; Fixed point Number System; Floating Point Number system - IEEE 754 format, Basic binary codes.

UNIT - II

Combinational circuits: CMOS logic design, Static and dynamic analysis of Combinational circuits, timing hazards.Functional blocks - Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, Subtractors, Carrylook- ahead adder – timing analysis. Combinational multiplier structures.

UNIT - III

Sequential Logic: Latches and Flip-Flops, Sequential logic circuits - timing analysis (Set up and hold times), State machines - Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; Synchronizers and meta stability. FSM Design examples: Vending machine, Traffic light controller, Washing machine.

UNIT - IV

Subsystem Design using Functional Blocks (1): Design (including Timing Analysis) of different logical blocks of varying complexities involving mostly combinational circuits:

- ALU
- 4-bit combinational multiplier
- Barrel shifter
- Simple fixed point to floating point encoder
- Dual Priority encoder
- Cascading comparators

UNIT - V

Subsystem Design using Functional Blocks (2): Design, (including Timing Analysis) of different logical blocks of different complexities involving mostly sequential circuits:

- Pattern (sequence) detector
- Programmable Up-down counter

- Round robin arbiter with 3 requesters Process Controller
- FIFO

TEXT BOOKS:

1. John F. Wakerly, "Digital Design", Prentice Hall, 3rd Edition, 2002.

REFERENCE BOOKS:

1. Behrooz Parhami, "Computer Arithmetic: Algorithms and Hardware Designs", Oxford University Press,2000.
2. M Morris Mano, "Digital Logic and Computer Design", Pearson Education India; 3 edition ,2007.

*Note1: VHDL and ABEL are not part of this course.

*Note2: SSI & MSI ICs listed in data books are not part of this course.

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M. Tech – I Year – I Sem	**L**	**P**	**C**
	4	**0**	**4**

VLSI DESIGN VERIFICATION AND TESTING (PC-2)

UNIT-I

Introduction to Verilog HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, Systems tasks, programming language interface, Module, Simulation and Synthesis tools.

Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic values, Strengths, Data types, Scalars and Vectors, Parameters, Operators.

UNIT-II

Verilog/VHDL Comparisons and Guidelines, Verilog: HDL fundamentals, simulation, and test- bench design, Examples of Verilog codes for combinational and sequential logic, Verilog AMS

UNIT-III

System Verilog and Verification: Verification guidelines, Data types, procedural statements and routines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization, Introduction to basic scripting language: Perl, Tcl/Tk

UNIT-IV

Advanced System Verilog: Callbacks, Parameterized Classes, Static and Singleton Classes Coverage: Introduction, Coverage Types, Functional Coverage Strategies, cover group, defining cover groups in classes, Data sampling, coverage points, Coverage methods, Cross coverage, Case study using Universal Verification Machine (UVM).

UNIT-V

Current challenges in physical design: Roots of challenges, Delays: Wire load models Generic PD flow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop, Process effects: Process Antenna Effect & Electromigration

TEXTBOOKS:

1. Douglas Smith, "HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog", Doone publications, 1998.
2. Samir Palnitkar, "Verilog HDL: A guide to Digital Design and Synthesis", Prentice Hall, 2nd Edition, 2003.

3. Christ Spear and Greg Tumbush, “System Verilog for Verification”, 3rd ed., Springer, 2012.

REFERENCES:

1. Ming-Bo Lin., “Digital System Designs and Practices Using Verilog HDL and FPGAs”, Wiley India, 2008.
2. Christophe Bobda, “Introduction to Reconfigurable Computing, Architectures, Algorithms and Applications”, Springer, 2007.
3. Janick Bergeron, “Writing Testbenches: Functional Verification of HDL Models”, Second Edition, Springer, 2003

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M. Tech – I Year – I Sem	**L**	**P**	**C**
	4	**0**	**4**

CMOS ANALOG INTEGRATED CIRCUIT DESIGN (PC-3)

UNIT -I

MOS Devices and Modeling: The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, International 2nd Edition/Indian Edition, 2010.
2. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley India, 5th Edition, 2010.

REFERENCE BOOKS:

1. David A. Johns, Ken Martin, "Analog Integrated Circuit Design", Wiley Student, Edition,2013.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH Edition.
3. Baker, Li and Boyce, "CMOS: Circuit Design, Layout and Simulation", PHI.

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M. Tech – I Year – I Sem

L	P	C
3	0	3

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN (PE-1)

UNIT –I:

MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II:

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI andOIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:

Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:

Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOStransmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:

Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

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M. Tech – I Year – I Sem	**L**	**P**	**C**
	3	**0**	**3**

HARDWARE SOFTWARE CO-DESIGN (PE-1)

UNIT –I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications andmulti-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, "Hardware / Software Co- Design Principles and Practice", Wayne Wolf – 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co-Design", 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. Patrick R. Schaumont, "A Practical Introduction to hardware/Software Co-design", 2010, Springer

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M. Tech – I Year – I Sem	**L**	**P**	**C**
	3	**0**	**3**

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (PE-1)

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices –Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer International Edition.
2. Charles H. Roth Jr, Lizy Kurian John, "Digital Systems Design", Cengage Learning.

REFERENCE BOOKS:

1. John V. Oldfield, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley India.
2. Pak K. Chan/Samiha Mourad, "Digital Design Using Field Programmable Gate Arrays", Pearson Low Price Edition.
3. Ian Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier,Newnes.
4. Wayne Wolf, "Modern Semiconductor Design Series", Prentice Hall.

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M. Tech – I Year – I Sem	**L**	**P**	**C**
	3	**0**	**3**

ALGORITHMS FOR VLSI DESIGN AUTOMATION (PE-2)

UNIT- I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems**.**

UNIT -II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT- III

LAYOUT COMPACTION, PLACEMENT, FLOOR PLANNING AND ROUTING: Problems, Concepts
and Algorithms.

MODELLING AND SIMULATION: Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT -IV

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT- V

PHYSICAL DESIGN AUTOMATION OF FPGAs: FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs : MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", 1999, WILEY Student Edition, John Wiley & Sons (Asia) Pvt. Ltd.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation",
   3rd Edition, 2005, Springer International Edition.

REFERENCE BOOKS:

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", 1993, Wiley.
2. Wayne Wolf, "Modern VLSI Design: Systems on silicon", 2nd ed., 1998, Pearson Education Asia.

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M. Tech – I Year – I Sem	**L**	**P**	**C**
	3	**0**	**3**

EMBEDDED SYSTEM DESIGN (PE-2)

UNIT -I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Shibu K.V, "Introduction to Embedded Systems", McGraw Hill.

REFERENCE BOOKS:

1. Raj Kamal, "Embedded Systems", TMH.
2. Frank Vahid, Tony Givargis, "Embedded System Design", John Wiley
3. Lyla, "Embedded Systems", Pearson, 2013
4. David E. Simon, "An Embedded Software Primer", Pearson Education.

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M. Tech – I Year – I Sem

L	P	C
3	0	3

ADVANCED COMPUTER ARCHITECTURE (PE-2)

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance ,Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues ininter connecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design :Fundamentals of Super Scalar Processors",
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", McGraw Hill.,
3. Dezso Sima, Terence Fountain, Peter Kacsuk , "Advanced ComputerArchitecture - A Design Space Approach", Pearson Education.

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M. Tech – I Year – I Sem	**L**	**P**	**C**
	0	**3**	**2**

DIGITAL IC DESIGN LAB

Note:
Minimum of 10 experiments should be conducted and any 8 experiments from Part –I and 2experiments from Part –II.

Part –I: VLSI Front End Design:

Programming can be done using any complier and the design and implement on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK,T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment, Multiplication, and Division.
15. Design of Finite State Machine.

Part –II: VLSI Back End Design:

Design and implementation of CMOS digital circuits using Cadence/Mentor Graphics / Synopsys / Equivalent CAD tools.

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - Basic logic gates
   - CMOS inverter
   - CMOS NOR/ NAND gates

- CMOS XOR and MUX gates
- CMOS 1-bit full adder
- Static / Dynamic logic circuit (register cell)
- Latch
- Pass transistor

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths

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M. Tech – I Year – II Sem	**L**	**P**	**C**
	4	**0**	**4**

LOW POWER VLSI DESIGN (PC - 4)

UNIT – I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT – II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits,
MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT – III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT – IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT – V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits – Analysis and Design", TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.

REFERENCE BOOKS:

1. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press, 2011
2. Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press/Wiley International, 1998.
3. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley & Sons, 2000.
4. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.
5. A. Bellamour, M. I. Elamasri, "Low Power CMOS VLSI Circuit Design", Kluwer Academic Press, 1995.
6. Siva G. Narendran, Anatha Chandrakasan, "Leakage in Nanometer CMOS Technologies" Springer, 2005.

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	4	**0**	**4**

DESIGN FOR TESTABILITY (PC - 5)

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits" Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, "Digital Systems and Testable Design", Jaico Publishing House.
2. P.K. Lala, "Digital Circuits Testing and Testability", Academic Press.

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	4	**0**	**4**

FULL CUSTOM IC DESIGN (PC - 6)

UNIT - I

Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

UNIT - II

Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals

UNIT - III

Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

UNIT - IV

Layout considerations due to process constraints Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects.

UNIT - V

Proper layout CAD tools for layout, Planning tools, Layout generation tools, Support tools.

TEXT BOOKS:

1. Dan Clein, "CMOS IC Layout Concepts Methodologies and Tools", Newnes, 2000.
2. Ray Alan Hastings, "The Art of Analog Layout", 2nd Edition, Prentice Hall, 2006

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	3	**0**	**3**

VLSI AND DSP ARCHITECTURES (PE - 3)

UNIT - I

Essential feature of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance, Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls

UNIT - II

Data Path and Control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls

UNIT - III

Enhancing performance with pipeline: An overview of pipelining, a pipe lined data path. Pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

UNIT - IV

Computational Accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP system, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors,

D /A conversion errors

UNIT - V

Architectures for programmable digital signal processing devices: Introduction, basic architectural features, DSP Computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

TEXT BOOKS:

1. D. A, Patterson and J.L Hennessy, "Computer Organization and Design: Hardware/ Software Interface", 4th Ed., Elsevier, 2011
2. A. S Tannenbaum, "Structural Computer organization", 4th Ed., Prentice-Hall, 1999

REFERENCE BOOKS:

1. W. Wolf, "Modern VLSI Design: System on Silicon", 2nd Ed., Person Education,1998
2. Keshab Parhi, "VLSI Digital Signal Processing system design and implementations", Wiley 1999
3. Avatar sign, Srinivasan S, "Digital Signal Processing implementations using DSP microprocessors with examples", Thomson 4th reprint, 2004.

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CMOS MIXED SIGNAL CIRCUIT DESIGN (PE - 3)

UNIT - I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits-basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT - II

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT - III

Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT - IV

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT - V

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH Edition, 2002
2. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, International Second Edition/Indian Edition, 2010.
3. David A. Johns, Ken Martin, "Analog Integrated Circuit Design", Wiley Student Edition, 2013

REFERENCE BOOKS:

1. Rudy Van De Plassche, "CMOS Integrated Analog-to- Digital and Digital-to-Analog converters", Kluwer Academic Publishers, 2003
2. Richard Schreier, "Understanding Delta-Sigma Data converters", Wiley Interscience, 2005.
3. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", Wiley Interscience, 2009.

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DEVICE MODELING (PE - 3)

UNIT - I

MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Mid gap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation.

UNIT - II

MOS Capacitor Characteristics and Non idealities: CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges.

UNIT - III

The MOS transistor: Small signal modeling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.

UNIT - IV

The Bipolar transistor: Eber's-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics.

UNIT - V

FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.

TEXT BOOKS:

1. S. M. Sze, "Physics of Semiconductor Devices", 2nd Edition, Wiley Eastern, 1981.
2. Y. P. Tsividis, "Operation and Modelling of the MOS Transistor", McGraw-Hill, 1987.
3. E. Takeda, "Hot-carrier Effects in MOS Transistors", Academic Press, 1995.
4. P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer. 2009

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RF IC DESIGN (PE - 4)

UNIT – I

Introduction to RF and Wireless Technology: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

UNIT – II

Basic concepts in RF Design: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT – III

Multiple Access: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards.

Transceiver Architectures: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT – IV

Amplifiers, Mixers and Oscillators: LNAs, down conversion mixers, Cascaded Stages,oscillators, Frequency synthesizers.

UNIT – V

Power Amplifiers: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques.

TEXT BOOKS:

1. Behzad Razavi, RF Microelectronics Prentice Hall of India, 2001.
2. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits**,** Cambridge University Press.

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SYSTEM ON CHIP ARCHITECTURE (PE - 4)

UNIT – I

Introduction to the System Approach: System Architecture, Components of the system, Hardware Software, Processor Architectures, Memory, and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratch pads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, "Computer System Design System-on-Chip", Wiely India Pvt. Ltd.
2. Steve Furber, "ARM System on Chip Architecture", 2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Ricardo Reis, "Design of System on a Chip: Devices and Components", 1st Ed., 2004, Springer
2. Jason Andrews, "Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)", Newnes, BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques", 2001, Kluwer Academic Publishers.

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	3	**0**	**3**

SCRIPTING LANGUAGES (PE - 4)

UNIT - I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT - II

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT - III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT - IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT - V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. Java Script – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. David Barron, "The World of Scripting Languages", Wiley Student Edition, 2010.
2. Brent Welch, Ken Jones and Jeff Hobbs, "Practical Programming in Tcl and Tk", Fourth edition.
3. Herbert Schildt, "Java the Complete Reference", 7th Edition, TMH.

REFERENCE BOOKS:

1. Clif Flynt, "Tcl/Tk: A Developer's Guide", 2003, Morgan Kaufmann Series.
2. John Ousterhout, "Tcl and the Tk Toolkit", 2nd Edition, 2009, Kindel Edition.
3. WojciechKocjan and Piotr Beltowski, "Tcl 8.5 Network Programming book", Packt Publishing.
4. Bert Wheeler, "Tcl/Tk 8.5 Programming Cookbook", 2011, Packt Publishing Limited.

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ASIC CAD Lab

NOTE:
Minimum 10 experiments should be conducted and any 5 experiments from part -I and Part-II

Part-I: Design and implement the digital circuits using Mentor Graphics / Cadence/ Synopsys/Industry Equivalent Standard Software.

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. 8-bit Counter
4. Signed Pipelined Multiplier
5. Accumulator
6. Memory

Part-II: Design and implement the CMOS analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

1. Characteristics of NMOS & PMOS Transistor
2. Design of Common Source Amplifier with different Loads
3. Design of Single stage Cascode Amplifiers
4. Design of Current Mirrors
5. Design of Differential Amplifiers with Different Loads
6. Design of Two stage Opamp

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PRINCIPLES OF ELECTRONIC COMMUNICATIONS
(Open Elective-1)

UNIT - I

Introduction: Need for Modulation, Frequency translation, Electromagnetic spectrum, Gain, Attenuation and decibels.

UNIT - II

Simple description on Modulation: Analog Modulation-AM, FM, Pulse Modulation-PAM, PWM, PCM, Digital Modulation Techniques-ASK, FSK, PSK, QPSK modulation and demodulation schemes.

UNIT - III

Telecommunication Systems: Telephones Telephone system, Paging systems, Internet Telephony. **Networking and Local Area Networks:** Network fundamentals, LAN hardware, Ethernet LANs, Token Ring LAN.

UNIT - IV

Satellite Communication: Satellite Orbits, satellite communication systems, satellite subsystems, Ground Stations Satellite Applications, Global Positioning systems.

Optical Communication: Optical Principles, Optical Communication Systems, Fiber –Optic Cables, Optical Transmitters & Receivers, Wavelength Division Multiplexing.

UNIT - V

Cellular and Mobile Communications: Cellular telephone systems, AMPS, GSM, CDMA, WCDMA. **Wireless Technologies:** Wireless LAN, PANs and Bluetooth, ZigBee and Mesh Wireless networks, Wimax and MANs, Infrared wireless, RFID communication, UWB.

TEXT BOOKS

1. Louis E. Frenzel, "Principles of Electronic Communication Systems", 3rd Ed., McGraw Hill publications, 2008.
2. Kennady, Davis, "Electronic Communications systems", 4Ed., TMH, 1999

REFERENCE BOOKS

1. Tarmo Anttalainen, "Introduction to Telecommunications Network Engineering", Artech House Telecommunications Library.
2. Theodore Rappaport, "Wireless Communications-Principles and practice", Prentice Hall, 2002.
3. Roger L. Freeman, "Fundamentals of Telecommunications", 2 Ed. Wiley publications.
4. Wayne Tomasi, "Introduction to data communications and networking", Pearson Education, 2005.

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	3	**0**	**3**

EMBEDDED SYSTEM DESIGN
(Open Elective-2)

UNIT -I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Shibu K.V, "Introduction to Embedded Systems", McGraw Hill.

REFERENCE BOOKS:

1. Raj Kamal, "Embedded Systems", TMH.
2. Frank Vahid, Tony Givargis, "Embedded System Design", John Wiley.
3. Lyla, "Embedded Systems", Pearson, 2013
4. David E. Simon, "An Embedded Software Primer", Pearson Education.

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	3	**0**	**3**

PRINCIPLES OF COMPUTER COMMUNICATIONS AND NETWORKS (Open Elective–3)

UNIT - I

Overview of Computer Communications and Networking: Introduction to Computer Communications and Networking, Introduction to Computer Network, Types of Computer Networks, Network Addressing, Routing, Reliability, Interoperability and Security, Network Standards, The Telephone System and Data Communications.

UNIT - II

Essential Terms and Concepts: Computer Applications and application protocols, Computer Communications and Networking models, Communication Service Methods and data transmission modes, analog and Digital Communications , Speed and capacity of a Communication Channel, Multiplexing and switching, Network architecture and the OSI reference model.

UNIT - III

Analog and Digital Communication Concepts: Representing data as analog signals, representing data as digital signals, data rate and bandwidth reduction , Digital Carrier Systems.

UNIT - IV

Physical and data link layer Concepts: The Physical and Electrical Characteristics of wire, Copper media, fiber optic media, wireless Communications. Introduction to data link Layer, the logical link control and medium access control sub-layers.

UNIT - V

Network Hardware Components: Introduction to Connectors, Transreceivers and media convertors, repeaters, network interference cards and PC cards, bridges, switches, switches Vs Routers.

TEXT BOOKS:

1. Computer Communications and Networking Technologies, Michel A. Gallo and William H. Hancock, Thomson Brooks / Cole.

REFERENCE BOOKS:

1. Principles of Computer Networks and Communications, M. Barry Dumas, Morris Schwartz, Pearson.

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	3	**0**	**3**

INDUSTRIAL INSTRUMENTATION
(Open Elective–4)

UNIT - I

METROLOGY, VELOCITY AND ACCELERATION MEASUREMENT: Measurement of length - Gauge blocks – Plainness – Area using Simpson's rule, Plain meter – Diameter – Roughness – Angle using Bevel protractor, sine bars and Clinometer – Mechanical, Electrical, Optical and Pneumatic Comparators.Optical Methods for length and distance measurements using Optical flats and Michelson Interferometer.

Relative velocity – Translational and Rotational velocity measurements – Revolution counters and Timers - Magnetic and Photoelectric pulse counting stroboscopic methods. Accelerometers-different types, Gyroscopes-applications.

UNIT - II

FORCE AND PRESSURE MEASUREMENT: Force measurement – Different methods –Gyroscopic Force Measurement – Vibrating wire Force transducer. Basics of Pressure measurement –Manometer types – Force-Balance and Vibrating Cylinder Transducers – High and Low Pressure measurement – McLeod Gauge, Knudsen Gauge, Momentum Transfer Gauge, Thermal Conductivity Gauge, Ionization Gauge, Dual Gauge Techniques, Deadweight Gauges, Hydrostatic Pressure Measurement

UNIT - III

FLOW MEASUREMENT AND LEVEL MEASUREMENT: Flow Meters- Head type, Area type (Rota meter), electromagnetic type, Positive displacement type, mass flow meter, ultrasonic type, vertex shedding type, Hotwire anemometer type, Laser Doppler Velocity-meter. Basic Level measurements – Direct, Indirect, Pressure, Buoyancy, Weight, Capacitive Probe methods

UNIT - IV

DENSITY, VISCOSITY AND OTHER MEASUREMENTS: Density measurements – Strain Gauge load cell method – Buoyancy method - Air pressure balance method – Gamma ray method – Vibrating probe method. Units of Viscosity, specific gravity scales used in Petroleum Industries, Different Methods of measuring consistency and Viscosity –Two float viscorator – Industrial consistency meter. Sound-Level Meters, Microphones, Humidity Measurement

UNIT - V

CALIBRATION AND INTERFACING: Calibration using Master Sensors, Interfacing of Force, Pressure, Velocity, Acceleration, Flow, Density and Viscosity Sensors, Variable Frequency Drive

TEXT BOOKS:

1. Doeblin E.O., "Measurement Systems – Applications and Design", 4th Edition, McGraw Hill International, 1990.
2. Patranabis D, "Principles of Industrial Instrumentation", TMH. End edition 1997

REFERENCES:

1. Considine D. M., "Process Instruments and Control Handbook", 4th Edition, McGraw Hill International, 1993
2. Jain R.K., "Mechanical and Industrial Measurements", Khanna Publications.