Program Structure and Syllabus of Minors in VLSI Circuit Design

ELECTRONICS & COMMUNICATION ENGINEERING (ECE)

AR25_Regulations

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Minors in VLSI Circuit Design

Curriculum Structure

S.No	Course Code	Course Name	Credit Scheme			
			Lecture	Tutorial	Practical	Total
1	EH25010	Digital Electronic circuits (MOOCs)	3	-	2	4
2	EH25011	Hardware Design using Verilog	3	-	-	3
3	EH25012	VLSI design flow: RTL to GDS (MOOCs)	3	-	2	4
4	EH25013	Analog VLSI Design (MOOCs)	3	-	2	4
5	EM25014	Low Power VLSI Design (MOOCS)	3	-	-	3
	Total Credits		**15**	**00**	**06**	**18**

Note:

If MOOCs courses are not available for any reason on SWAYAM/NPTEL or any notified certification examinations, student shall register for a university-conducted examination for 100 marks through self-paced learning.

Digital Electronic Circuits

Minor Degree in VLSI Circuit Design					Department of Electronics & Communication Engineering			
Code	**Category**	**Hours / Week**			**Credits**	**Marks**		
EH25010	Core	L	T	P	C	CIE	SEE	Total
		3	0	2	4	-	100	100

Pre-Requisites: Basic understanding of diode, transistor operation and basic electronics or analog electronic circuit's course.

Course outline: This course is aimed at developing a deep understanding of digital electronic circuits. At the end of the course, one would be able to analyze and synthesize different kind of combinatorial and sequential digital systems for real-world use.

Course Plan

Week 1 : Introduction; Relation between switching and logic operation; Use of Diode and Transistor as switch; Concept of noise margin, fanout, propagation delay; TTL, Schottky TTL, Tristate; CMOS Logic, Interfacing TTL with CMOS.

Week 2: Basic logic gates, Universality of NAND, NOR gates, AND-OR-Invert gates, Positive and Negative Logic; Boolean Algebra axioms and basic theorems; Standard and canonical representations of logic functions, Conversion between SOP and POS; Simplification of logic functions, Karnaugh Map, Don't Care Conditions.

Week 3 : Minimization using Entered Variable Map, Minimization using QM algorithm; Cost criteria, Minimization of multiple output functions; Static-0, Static-1 and Dynamic Hazards and their cover.

Week 4: Multiplexer; Demultiplexer / Decoder, BCD to 7-segment decoder driver; Encoder, Priority encoder; Parity generator and checker.

Week 5: Number systems-binary, Signed binary, Octal, hexadecimal number; Binary arithmetic, One's and two's complements arithmetic; Codes, Code converters; Adder, Subtractor, BCD arithmetic

Week 6: Carry look ahead adder; Magnitude comparator; ALU; Error detecting and correcting codes

Week 7: Bistable latch, SR, D, JK, T Flip-Flop: level triggered, edge triggered, master – slave, Various representations of flip-flops; Analysis and synthesis of circuits that use flip-flop.

Week 8: Register, Shift register, Universal shift register; Application of shift register: ring counter, Johnson counter, sequence generator and detector, serial adder; Linear feedback shift register.

Week 9 : Up and down counter, Ripple (asynchronous) counters, Synchronous counters; Counter design using flip flops, Counter design with asynchronous reset or preset; Applications of counters.

Week 10: Design of synchronous sequential circuit using Mealy model and Moore model: state transition diagram, algorithm state machine (ASM) chart; State reduction technique

Week 11: Digital to analog converters: weighted resistor/converter, binary ladder, converter, accuracy and resolution; Analog to digital converter: quantization and encoding, different types of conversion, accuracy and resolution.

Week 12: Memory organization and operation, Memory expansion; Memory cell; Different types of memory, ROM, PROM, PAL, PLA, CPLD, FPGA.

Practical Assessment:
Based on the course content, the Faculty Mentor will assign problem sets for students to solve and submit. Marks are awarded according to the quality of the submitted work.

Hardware Design using Verilog

Minor Degree in VLSI Circuit Design					Department of Electronics & Communication Engineering			
Code	**Category**	**Hours / Week**			**Credits**	**Marks**		
EH25011	Core	L	T	P	C	CIE	SEE	Total
		3	0	0	3	-	100	100

Pre-Requisites: Basic concepts in digital circuit design; Familiarity with a programming language like C or C++

Course objectives:

- Concepts of VLSI design flow, Verilog basics.
- Concepts of Verilog constructs, Verilog description styles.
- Methods like switch level modelling, Synthesize
- Concepts of combinational and sequential design.

Course Content

Unit 1: Introduction to digital circuit design flow: VLSI design flow, design representation, Verilog basics, VLSI design styles.

Unit 2: Verilog HDL: Verilog language features, Verilog Description styles, Procedural assignments, blocking and non-blocking assignments, Verilog test benches and simulation

Unit 3: Data path and Controller design, Synthesizable Verilog, switch-level modelling.

Unit 4: Synthesis of combinational logic using Verilog**:** Half adder, full adder and ripple carry adder, Parallel adder/subtractor, Multiplier and comparator, Decoder, encoder, and multiplexer, Demultiplexer.

Unit 5: Synthesis of sequential logic using Verilog: Flipflops, shift registers, counters, sequence detectors.

Books and references:

1. Design through Verilog HDL-T. R. Padmanabhan and B. Bala Tripura Sundari; WSE, IEEE Press, 2004
2. Advanced Digital Design with Verilog HDL- Michael D. Ciletti, PHI, 2005

Course Outcomes:

Students will be able to:

1. Use VLSI design methodologies to understand and design of digital systems.
2. Develop HDL for basic logic gates that realize specified digital functions.
3. Synthesize the data path and control systems
4. Design and synthesize the combinational logic circuits
5. Design and synthesize the sequential logic circuits.

VLSI Design Flow: RTL to GDS

Minor Degree in VLSI Circuit Design					Department of Electronics & Communication Engineering			
Code	**Category**	**Hours / Week**			**Credits**	**Marks**		
EH25012	Core	L	T	P	C	CIE	SEE	Total
		3	0	2	4	-	100	100

Pre-Requisites: Basic Course on Digital Circuits (typically taught in the first/second year of UG Program)

Course outline: This course covers the entire RTL to GDS VLSI design flow, going through various stages of logic synthesis, verification, physical design, and testing. Besides covering the fundamentals of various design tasks, this course will develop skills in modern chip design with the help of activities and demonstrations on freely available CAD tools. This course will enhance the employability of the students and will make them ready to undertake careers in the semiconductor industry.

Course Plan

Week 1: Basic Concepts of Integrated Circuit: Structure, Fabrication, Types, Design Styles, Designing vs. Fabrication, Economics, Figures of Merit Overview of VLSI Design Flow: Design Flows and Abstraction; Pre-RTL Methodologies: Hardware-software Partitioning, SoC Design, Intellectual Property (IP) Assembly, Behavioral Synthesis

Week 2: Overview of VLSI Design Flow: RTL to GDS Implementation: Logic Synthesis, Physical Design; Verification and Testing; Post-GDS Processes.

Week 3: Hardware Modeling: Introduction to Verilog Functional verification using simulation: testbench, coverage, mechanism of simulation in Verilog

Week 4: RTL Synthesis: Verilog Constructs to Hardware Logic Optimization: Definitions, Two-level logic optimization

Week 5: Logic Optimization: Multi-level logic optimization, FSM Optimization Formal Verification: Introduction, Formal Engines: BDD, SAT Solver

Week 6: Formal Verification: Model Checking, Combinational Equivalence Checking Technology Library: Delay models of Combinational and Sequential Cells

Week 7: Static Timing Analysis: Synchronous Behavior, Timing Requirements, Timing Graph, Mechanism, Delay Calculation, Graph-based Analysis, Path-based Analysis, Accounting for Variations

Week 8: Constraints: Clock, I/O, Timing Exceptions Technology Mapping Timing-driven Optimizations

Week 9: Power Analysis, Power-driven Optimizations Design for Test: Basics and Fault Models, Scan Design Methodology

Week 10: Design for Test: ATPG, BIST Basic Concepts for Physical Design: IC Fabrication, FEOL, BEOL, Interconnects and Parasitics, Signal Integrity, Antenna Effect, LEF files

Week 11: Chip Planning: Partitioning, Floorplanning, Power Planning Placement: Global Placement, Wirelength Estimates, Legalization, Detailed Placement, Timing-driven Placement, Scan Cell Reordering, Spare Cell Placement

Week 12: Clock Tree Synthesis: Terminologies, Clock Distribution Networks, Clock Network Architectures, Useful Skews Routing: Global and Detailed, Optimizations Physical Verification: Extraction, LVS, ERC, DRC, ECO and Sign-off.

Practical Assessment:

Based on the course content, the Faculty Mentor will assign problem statements for students to implement using any supported CAD tool. Marks are awarded according to the performance of the submitted work.

Analog VLSI Design

Minor Degree in VLSI Circuit Design					Department of Electronics & Communication Engineering			
Code	**Category**	**Hours / Week**			**Credits**	**Marks**		
EH25013	Core	L	T	P	C	CIE	SEE	Total
		3	0	2	4	-	100	100

Pre-Requisites: Network theory, Laplace transform, Sinusoidal state analysis

Course outline: This course is aimed at introducing analog circuits from the perspective of designing amplifiers in an integrated circuit using MOS transistors. The students will be introduced to the techniques required for designing amplifiers using negative feedback as the guiding principle. Small signal characteristics of widely used amplifier topologies will be discussed and their limitations analysed. The learning objective of the course is to make the students proficient in the synthesis basic amplifier topologies so that one can develop an intuition to design circuits based on specific requirements in their career.

Course Plan

Week 1 & 2 : Introduction: Linearization of non-linear elements, Generation of small incremental linear equivalents from non-linear elements.

Week 3 & 4 : Basic amplifier design using MOSFET. Common source amplifier with resistive load.Biasing a common source amplifier. Gain limitations of the configuration.Introduction to swing limits. Relevance of the limitations in a integrated circuit.

Week 5 & 6 : Different biasing techniques of a common source amplifier. Use of negative feedback to realize stable biasing. Distinction between constant voltage and constant current biasing.

Week 7 & 8 : Introduction to controlled sources. Realizing controlled sources using a voltage controlled current source. Using MOSFETs to realize the controlled sources and other amplifier configurations. Body effects in an MOSFET. The effect of output resistance of a MOSFET on an amplifier configuration.

Week 9 & 10 : Introduction to active loads, and single stage differential amplifiers. Analysis of gain,swing limits, slew rate, common mode rejection ratio, power supply rejection ratio in a single stage differential amplifier.

Week 11 & 12 : Multi-stage amplifiers using controlled sources. Introduction of stability parameters of multistage amplifier when configured in negative feedback. Design and analysis of multi-stage amplifier by replacing the controlled sources with MOSFETs.

Practical Assessment:

Each student will deliver a seminar on a topic related to the course. Marks will be awarded based on the quality of the presentation and supporting materials.

Low Power VLSI Design

Minor Degree in VLSI Circuit Design					Department of Electronics & Communication Engineering			
Code	**Category**	**Hours / Week**			**Credits**	**Marks**		
EM25014	Core	L	T	P	C	CIE	SEE	Total
		3	0	0	3	-	100	100

Prerequisites: Digital circuits, VLSI design.

Course Objectives:

- To understand the necessity of low-power circuit design and various sources of power dissipation in CMOS transistors
- To learn the various low-power techniques like voltage scaling, architectural level approach, and switched capacitance minimization approach
- To apply the low-power technique for adder and multiplier design implementation
- To design and analyze low-power RAM and ROM memory cells

Course content

Unit 1: Introduction to low power design:

Need for low power circuit design, sources of power dissipation – Switching power dissipation, short circuit power dissipation, leakage power dissipation, glitching power dissipation, short channel effects –drain induced barrier lowering and punch through, surface scattering, velocity saturation, impact ionization, hot electron effect.

Unit 2: Low-Power Design Approaches:

Low-power design through voltage scaling – VTCMOS circuits, MTCMOS circuits, architectural level approach – pipelining and parallel processing approaches. switched capacitance minimization approaches: system level measures, circuit level measures, mask level measures.

Unit 3: Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder Architectures – ripple carry adders, carry look-ahead adders, carry select adders, carry save adders, low-voltage low-power design techniques –trends of technology and power supply voltage, low-voltage low-power logic styles.

Unit 4: Low-Voltage Low-Power Multipliers:

Introduction, overview of multiplication, types of multiplier architectures-braun multiplier, baugh-wooley multiplier, booth multiplier, wallace tree multiplier.

Unit 5: Low-Voltage Low-Power Memories:

Basics of ROM, low-power ROM technology, future trend and development of ROMs, Basics of SRAM, memory cell, precharge and equalization circuit, low-power SRAM technologies, basics of DRAM, self-refresh circuit, future trend and development of DRAM.

Text Books:

1. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and

Design”, New York: McGraw-Hill, Second Edition, 2011.

2. Yeo, Kiat-Seng, and Kaushik Roy,” Low voltage, low power VLSI subsystems”, McGraw-

Hill, Inc., 2004.

Reference Books

1. Ming-BO Lin, "*Introduction to VLSI Systems: A Logic, Circuit and System Perspective*", CRC Press, First Edition, 2012.
2. AnanthaChandrakasan, "*Low Power CMOS Design*", IEEE Press/Wiley International, First Edition, 1998.
3. Kaushik Roy, Sharat C. Prasad, "*Low Power CMOS VLSI Circuit Design*", John Wiley & Sons, First Edition, 2009.
4. Gary K. Yeap, "*Practical Low Power Digital VLSI Design*", Kluwer Academic Press, 2002.
5. A. Bellamour, M. I. Elamasri, "*Low Power CMOS VLSI Circuit Design*", Kluwer Academic Press, 1995.
6. Siva G. Narendran, AnathaChandrakasan, "*Leakage in Nanometer CMOS Technologies*" Springer, Third Edition, 2005.

Course Outcomes:

- After completing the course, students will be able to
- Understand about the sources of power dissipation and the necessity of low-power circuit design
- Analyze the low-power technique in different levels of circuits
- Design the low-power adder with various low-power techniques
- Apply various low-power architectures for low-power multiplier implementation
- Analyze the future trend and development of RAM and ROM cell for low-power design